

SuZhou

CPU : Intel Arrandale
Chip Set : Intel Ibex Peak(PM55)
GFX : N11P / M-GE(40nm)
Remarks : Calpella Platform

Model Name : SuZhou-MH
PBA Name : MAIN
PCB Code : BA41-01190A
Dev. Step : PVR
Revision : 1.0
T.R. Date : 2009.11.3

Design	CHECK	APPROVAL
Xiaohong Zhang	Rujin Zheng	BC Lee

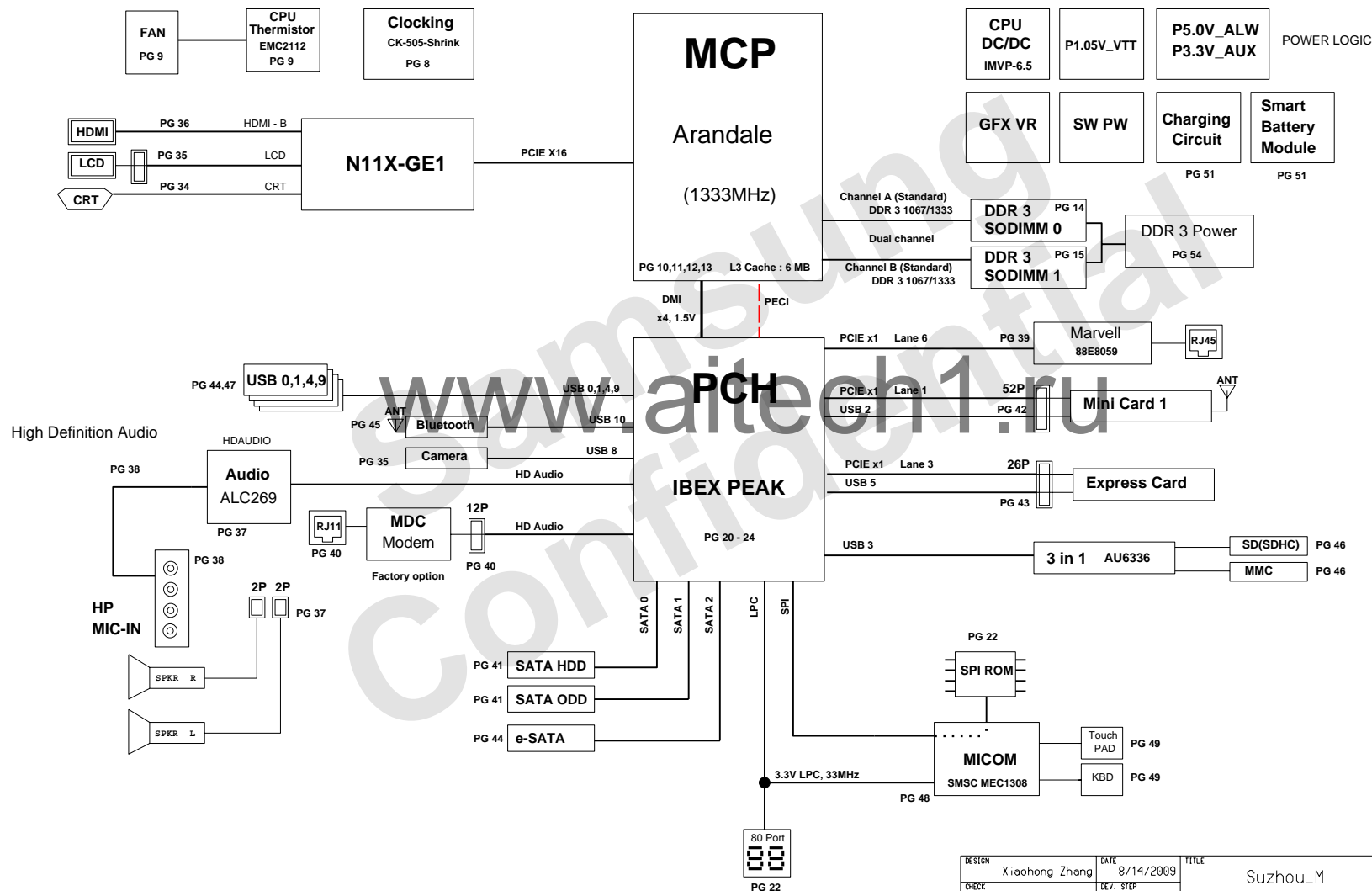
■ Owner : SEC Mobile R & D Signature : X

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DESIGN	Xiaohong Zhang	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
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BLOCK DIAGRAM



DESIGN	Xiaohong Zhang	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		UNDEFINED	
APPROVAL	BC LEE	REV	1.0		UNDEFINED	
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails	Active in
VDC P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)
P5.0V P3.3V P1.8V P1.5V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)
VCC_CORE EGFX_CORE P1.05V (VCCP) P1.1V_VTT	Core Voltage for CPU Core Voltage for GPU VCC for Clarkfield & IBEX Peak VTT for CLARDSFIELD & IBEX Peak

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN
Crystal	25MHz	IBEX PEAK	

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0
---------	------------	-----------------

IC / SMB Address

Devices	Address	Hex	Bus
IBEX-PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Mini PCI Express 1	3	EXPRESS CARD
3	NC	4	NC
4	SYSTEM PORT 4	5	NC
5	EXPRESS CARD	6	NC
6	NC (N/A WITH HM55)	7	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)	8	NC (N/A WITH HM55)
8	Multi Memory Card Controller		
9	SYSTEM PORT 9		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

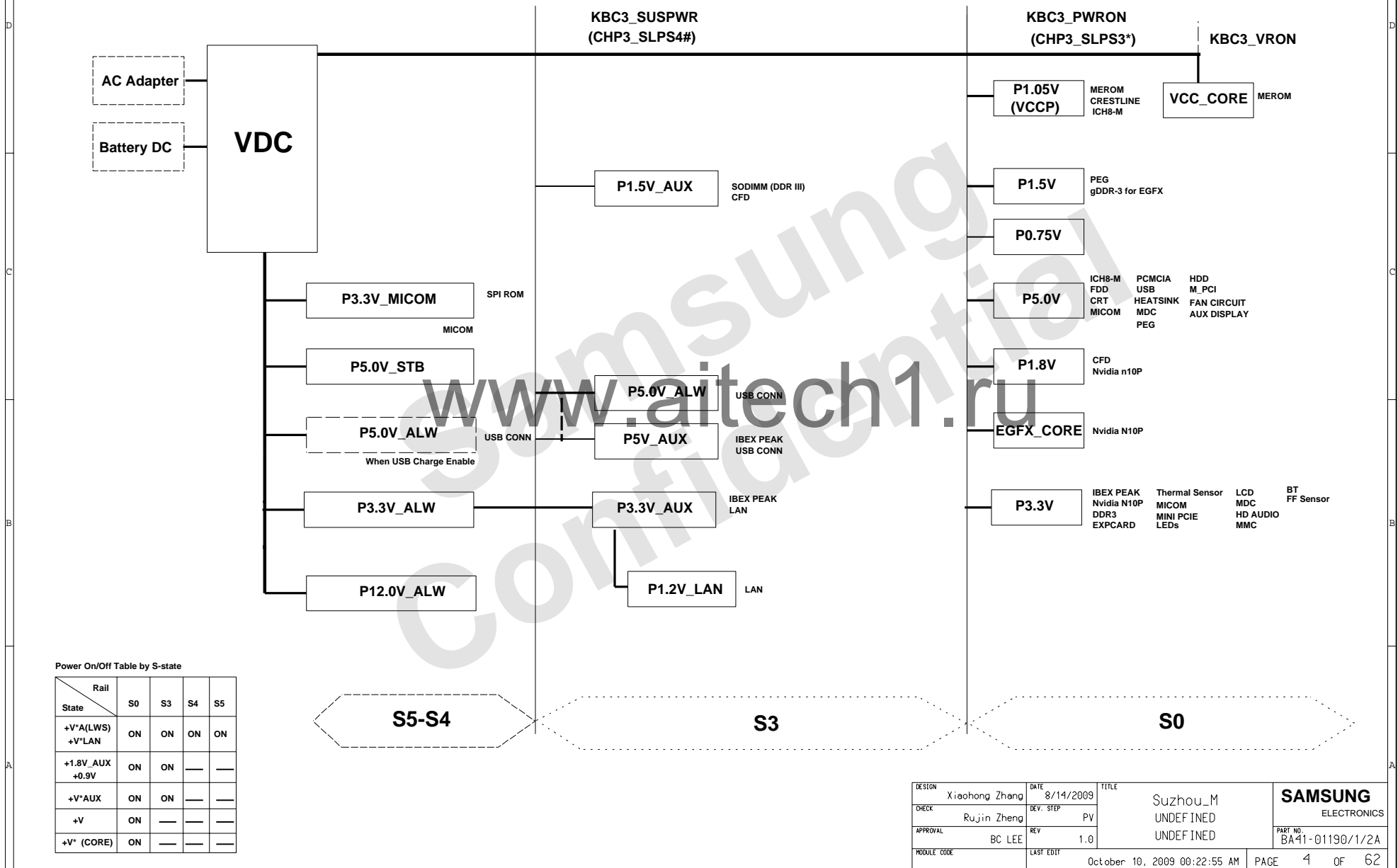
SATA PORT Assign

PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	e-SATA

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POWER DIAGRAM

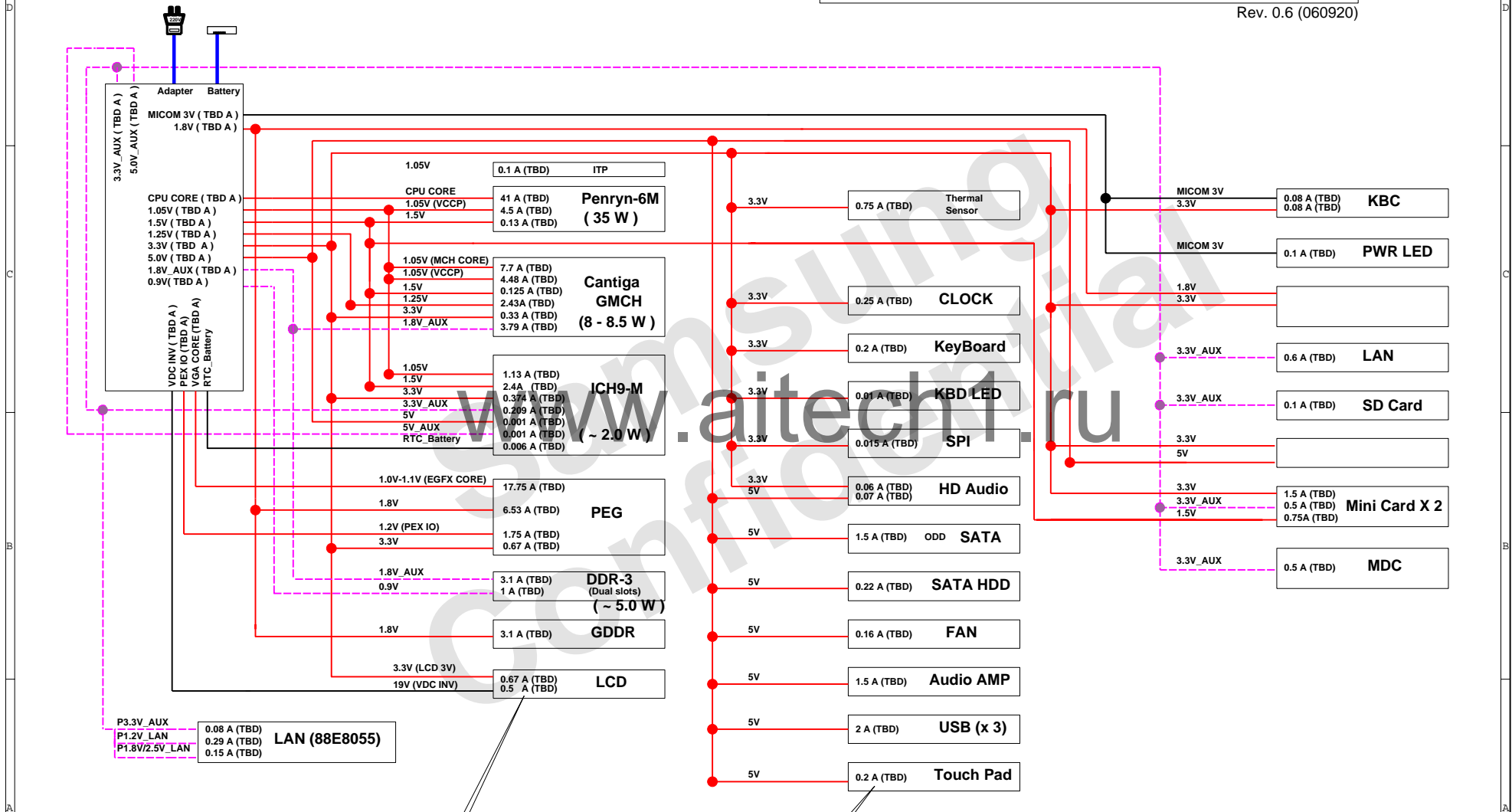
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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

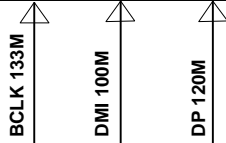


Value by Datasheet/Application notes (Value by measurement)

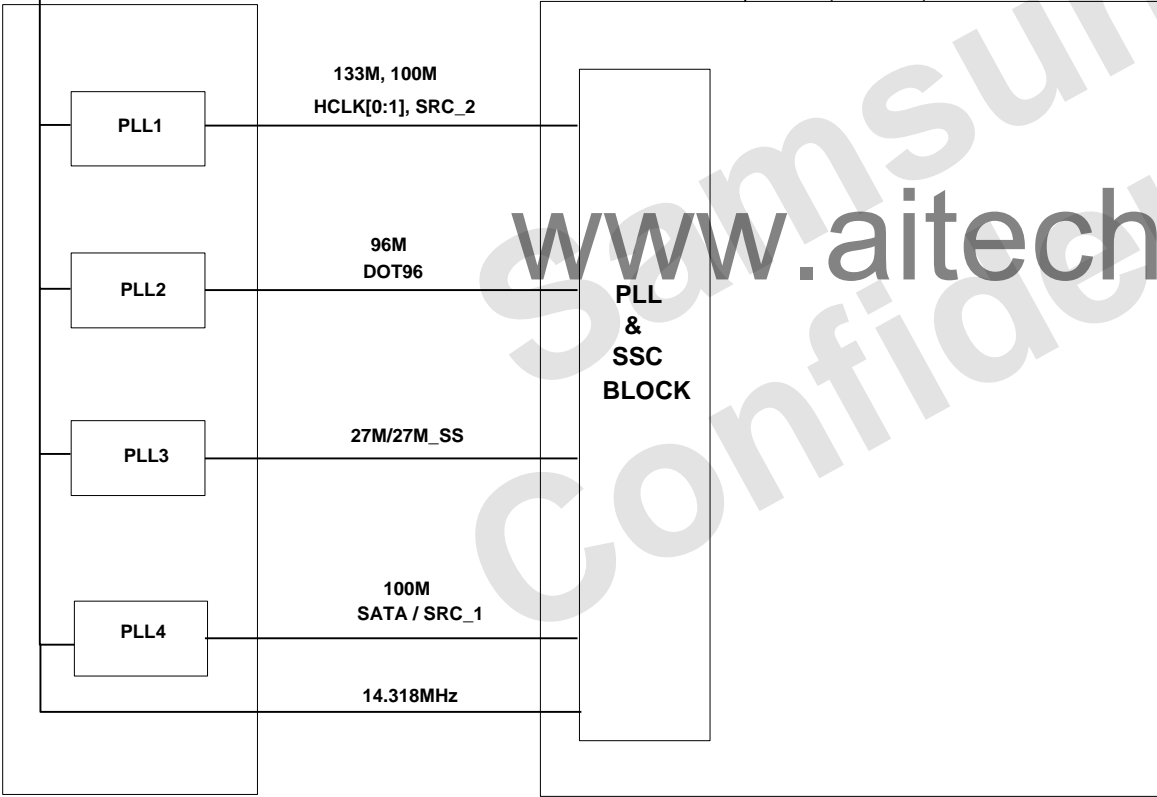
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CLOCK DISTRIBUTION Rev. 0.1



XTAL



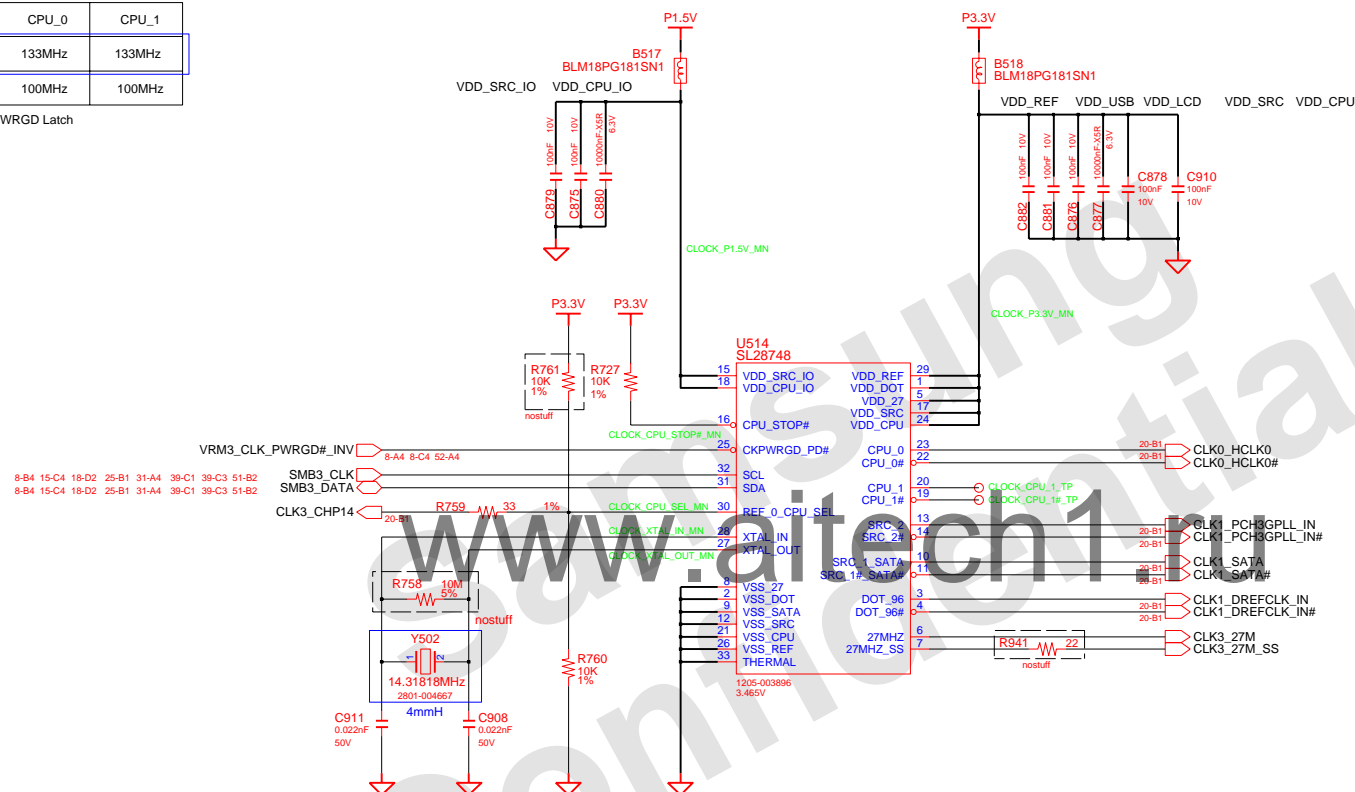
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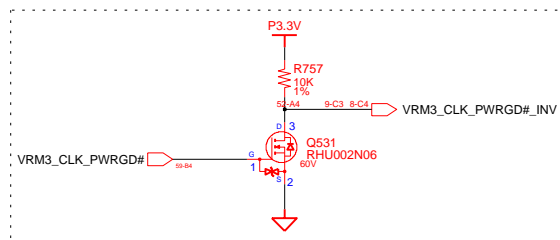
CPU_MODE_SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

*CPU_SEL During CK_PWRGD Latch



Place 14.318MHz within
500mils of CK-505



DRAW	Xiaohong Zhang	DATE	8/12/2006	TITLE Suzhou_M Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		
APPROVAL	BC LEE	REV	1.0		
MODULE CODE	undefined				
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THERMAL SENSOR & FAN CONTROL

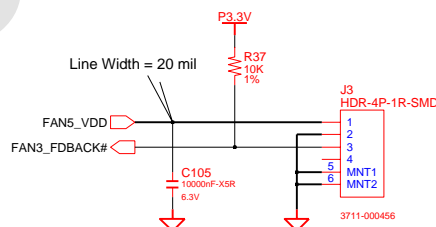
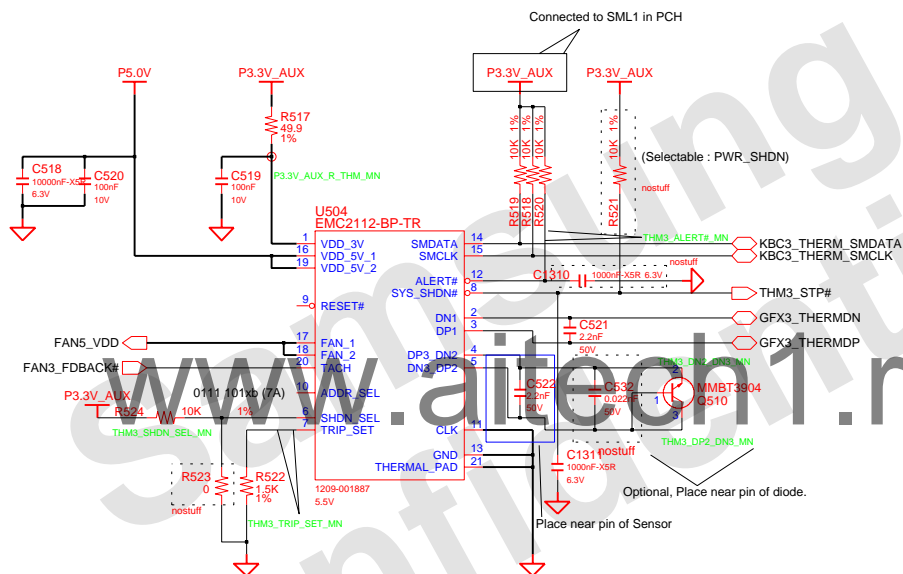
ADDRESSSEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

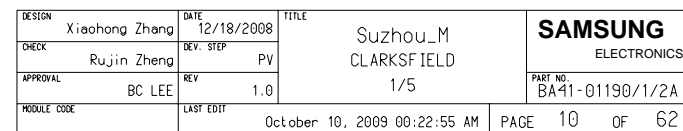
SHDN_SEL MODE	
0 HIGH Z	INTEL TR MODE AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

TRIP_SET Resistor Setting (60 ~ 122 C)	
60	0.0
95	1500
96	1580
97	1690
98	1820
99	1960
100	2050
101	2210
102	2370
✓ 103	2550
104	2740
105	2940
122	49900

$$V_Trip = (T_Trip - T_Min) / 80$$

V_TRIP : TRIP_SET Voltage
T_Min : Minimum Temperature

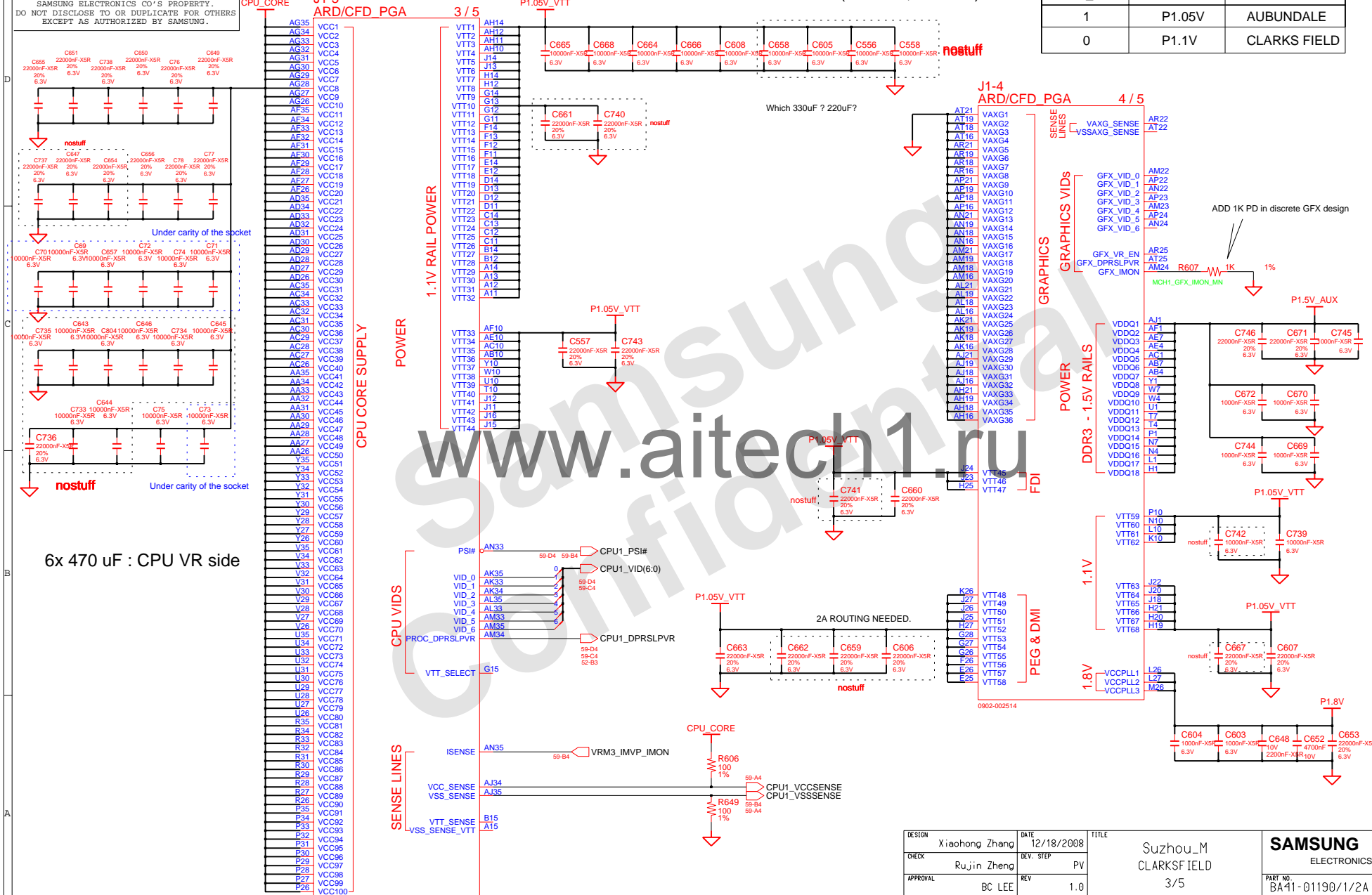




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ALL VTT DECAP IS SHARED(10uFX9, 22uFx7)

VTT_SEL	VOLTAGE	CPU
1	P1.05V	AUBUNDALE
0	P1.1V	CLARKS FIELD



DESIGN	Xiaohong Zhang	DATE	12/18/2008	TITLE	Suzhou_M CLARKSFIELD 3/5	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
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J1-5
ARD/CFD_PGA5 / 5

VSS47	VSS1	VSS81	AE34
AR17	VSS2	VSS82	AE35
AR31	VSS3	VSS83	AE36
AR28	VSS4	VSS84	AE37
AR26	VSS5	VSS85	AE38
AR24	VSS6	VSS86	AE39
AR23	VSS7	VSS87	AE40
AR20	VSS8	VSS88	AE41
AR17	VSS9	VSS89	AE42
AR15	VSS10	VSS90	AE43
AR12	VSS11	VSS91	AE44
AR9	VSS12	VSS92	AE45
AR6	VSS13	VSS93	AE46
AR3	VSS14	VSS94	AE47
AP20	VSS15	VSS95	AE48
AP17	VSS16	VSS96	AE49
AP13	VSS17	VSS97	AE50
AP10	VSS18	VSS98	AE51
AP7	VSS19	VSS99	AE52
AP2	VSS20	VSS100	AE53
AN34	VSS21	VSS101	AE54
AN31	VSS22	VSS102	AE55
AN23	VSS23	VSS103	AE56
AN20	VSS24	VSS104	AE57
AN17	VSS25	VSS105	AE58
AM29	VSS26	VSS106	AE59
AM27	VSS27	VSS107	AE60
AM25	VSS28	VSS108	AE61
AM20	VSS29	VSS109	AE62
AM17	VSS30	VSS110	AE63
AM14	VSS31	VSS111	AE64
AM11	VSS32	VSS112	AE65
AM8	VSS33	VSS113	AE66
AM5	VSS34	VSS114	AE67
AM2	VSS35	VSS115	AE68
AL34	VSS36	VSS116	AE69
AL31	VSS37	VSS117	AE70
AL23	VSS38	VSS118	AE71
AL20	VSS39	VSS119	AE72
AL17	VSS40	VSS120	AE73
AL12	VSS41	VSS121	AE74
AL9	VSS42	VSS122	AE75
AL6	VSS43	VSS123	AE76
AL3	VSS44	VSS124	AE77
AK29	VSS45	VSS125	AE78
AK27	VSS46	VSS126	AE79
AK25	VSS47	VSS127	AE80
AK20	VSS48	VSS128	AE81
AK17	VSS49	VSS129	AE82
AK11	VSS50	VSS130	AE83
AK31	VSS51	VSS131	AE84
AK23	VSS52	VSS132	AE85
AK20	VSS53	VSS133	AE86
AK14	VSS54	VSS134	AE87
AK11	VSS55	VSS135	AE88
AK8	VSS56	VSS136	AE89
AK5	VSS57	VSS137	AE90
AK2	VSS58	VSS138	AE91
AK3	VSS59	VSS139	AE92
AK35	VSS60	VSS140	AE93
AK34	VSS61	VSS141	AE94
AK33	VSS62	VSS142	AE95
AK32	VSS63	VSS143	AE96
AK31	VSS64	VSS144	AE97
AK30	VSS65	VSS145	AE98
AK29	VSS66	VSS146	AE99
AK28	VSS67	VSS147	AE100
AK27	VSS68	VSS148	AE101
AK26	VSS69	VSS149	AE102
AK25	VSS70	VSS150	AE103
AK24	VSS71	VSS151	AE104
AK23	VSS72	VSS152	AE105
AK22	VSS73	VSS153	AE106
AK21	VSS74	VSS154	AE107
AK20	VSS75	VSS155	AE108
AK19	VSS76	VSS156	AE109
AK18	VSS77	VSS157	AE110
AK17	VSS78	VSS158	AE111
AK16	VSS79	VSS159	AE112
AK15	VSS80	VSS160	AE113

0002-002514

K27	VSS161
K9	VSS162
K6	VSS163
K3	VSS164
J32	VSS165
J30	VSS166
J21	VSS167
J19	VSS168
H35	VSS169
H32	VSS170
H26	VSS171
H22	VSS172
H18	VSS173
H15	VSS174
H13	VSS175
H11	VSS176
H8	VSS177
H5	VSS178
H2	VSS179
G34	VSS180
G31	VSS181
G20	VSS182
G9	VSS183
G6	VSS184
G3	VSS185
F30	VSS186
F27	VSS187
F25	VSS188
F22	VSS189
F19	VSS190
F16	VSS191
F13	VSS192
F10	VSS193
F7	VSS194
F4	VSS195
E32	VSS196
E29	VSS197
E24	VSS198
E21	VSS199
E18	VSS200
E13	VSS201
E11	VSS202
E8	VSS203
E5	VSS204
E2	VSS205
D33	VSS206
D30	VSS207
D26	VSS208
D23	VSS209
D20	VSS210
D17	VSS211
D14	VSS212
D11	VSS213
D8	VSS214
D5	VSS215
D2	VSS216
C32	VSS217
C29	VSS218
C26	VSS219
C23	VSS220
C20	VSS221
C19	VSS222
C16	VSS223
C13	VSS224
C10	VSS225
C7	VSS226
C4	VSS227
C1	VSS228
B35	VSS229
B32	VSS230
B29	VSS231
B26	VSS232
B23	VSS233

VSS

NCTF

AT35
AT1
AR34
B34
B2
B1
A35
CPU_VSS_NCTF3
CPU_VSS_NCTF4
CPU_VSS_NCTF5

R650
3.01K 1%
CPU_CFG_7_R_MN

CPU_RSVD17_TP
CPU_RSVD18_TP

AP25	RSVD1	AJ13
AL25	RSVD2	AJ12
AL24	RSVD3	AH25
AL22	RSVD4	AK26
RSVD5	RSVD34	
RSVD6	RSVD35	
RSVD7	RSVD36	AL26
RSVD8	RSVD_NCTF_37	AR2
SA_DIMM_VREFDQ	RSVD38	AJ26
SB_DIMM_VREFDQ	RSVD39	AJ27
G25	RSVD11	
RSVD12	RSVD_NCTF_40	AP1
RSVD13	RSVD_NCTF_41	AT2
RSVD14	RSVD_NCTF_42	AT3
	RSVD_NCTF_43	AR1
AM30	CFG_0	AL28
AM28	CFG_1	AL29
AP31	CFG_2	AP30
AL32	CFG_3	AP32
AL30	CFG_4	AL27
AM31	CFG_5	AT31
AM29	CFG_6	AT32
AM32	CFG_7	AP33
AK32	CFG_8	AR33
AK31	CFG_9	AT33
AK28	CFG_10	AT34
AJ28	CFG_11	AP35
AK30	CFG_12	AR35
H16	CFG_13	AR32
B19	CFG_14	E15
A19	CFG_15	F15
A20	CFG_16	A2
B20	CFG_17	D15
U8	CFG_18	C15
T9	CFG_19	AJ15
AC9	CFG_20	AH15
AB9	CFG_21	
C1	CFG_22	
A3	CFG_23	
J29	CFG_24	
J28	CFG_25	
A34	CFG_26	
A33	CFG_27	
C35	CFG_28	
B35	CFG_29	
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	CFG_99	
	CFG_100	

(VSS) RSVD86

CFG Straps for Processor

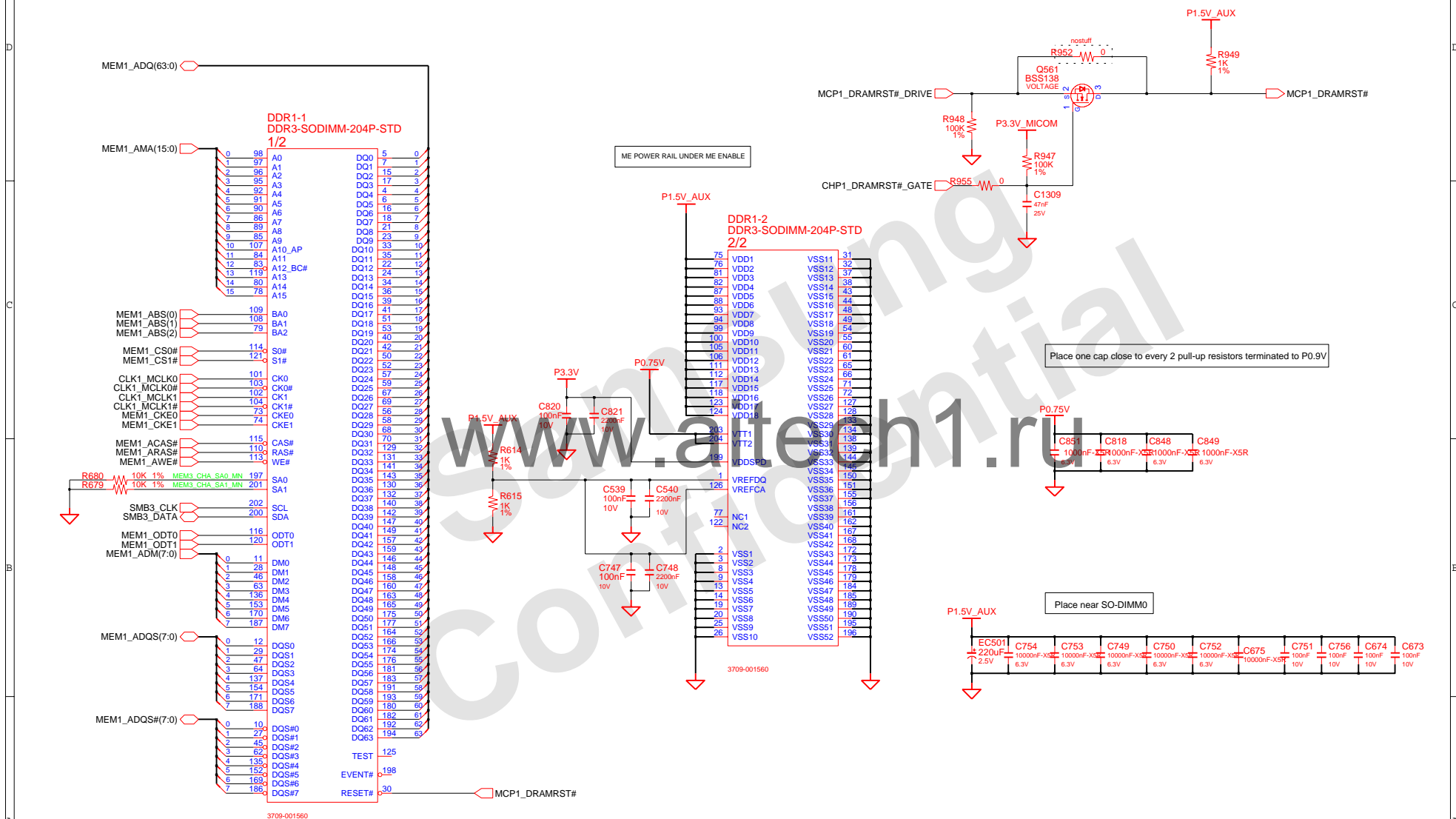
PCI Express Configuration Select		ALL nostuff
CFG0	1 : Single PEG 0 : Bifunction enabled	
PCI Express Static Lane Reversal		
CFG3	1 : Normal operation 0 : Lane Reversed	
Display Port Presence		
CFG4	1 : Disabled - No DP device is connected to eDP	
	0 : Enabled - (DP device is connected to eDP)	
PCIE 2.0 SUPPORT		
CFG7	1 : Normal operation 0 : PCIE2.0 Jitter support	

DESIGN	Xiaohong Zhang	DATE	12/18/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		CLARKSFIELD	
APPROVAL	BC LEE	REV	1.0		4/5	PART NO. BA41-01190/1/2A
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Height : 5.2mm (Reverse)

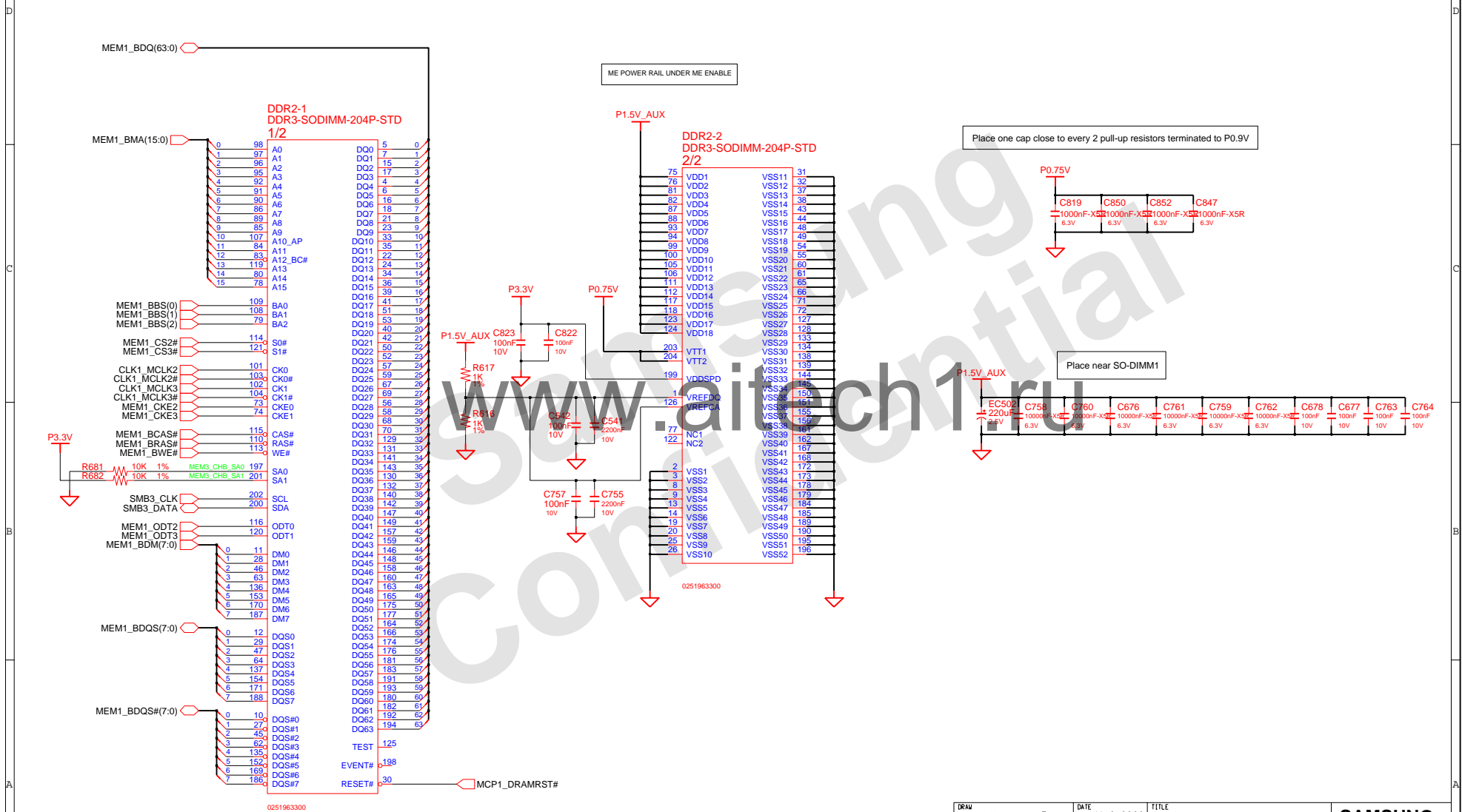
Height : 5.2mm (Reverse)



DRAW	Xiaohong Zhang	DATE	11/8/2006	TITLE	Suzhou_M SODIMM_REV DDR3 CH A	SAMSUNG ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP	PV			PART NO.	BA41-01190/1/2A
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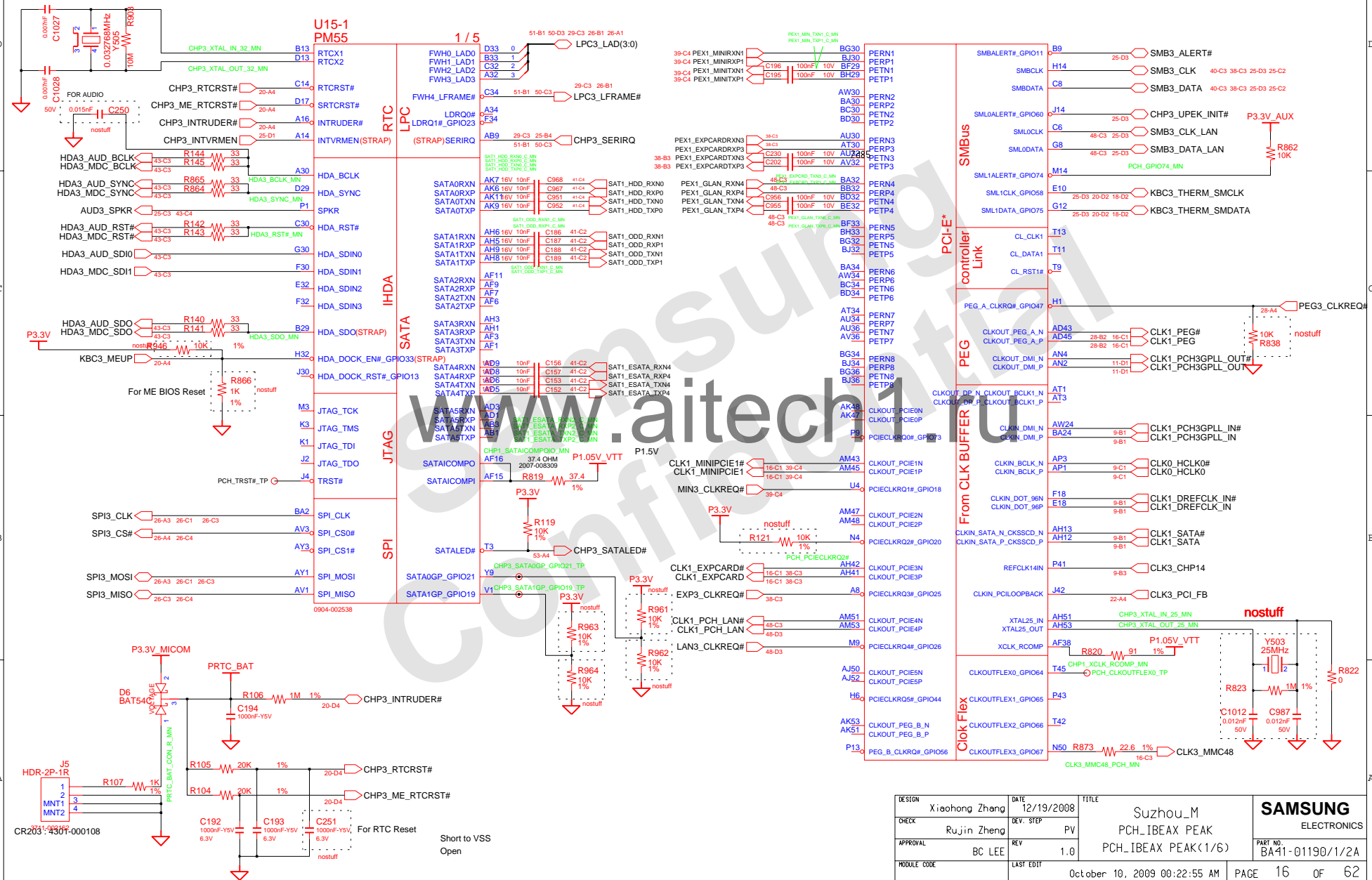
DDR SO-DIMM #1

Height : 9.2mm (Reverse)



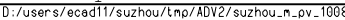
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CHECK	Rujin Zheng	DEV. STEP	PV			
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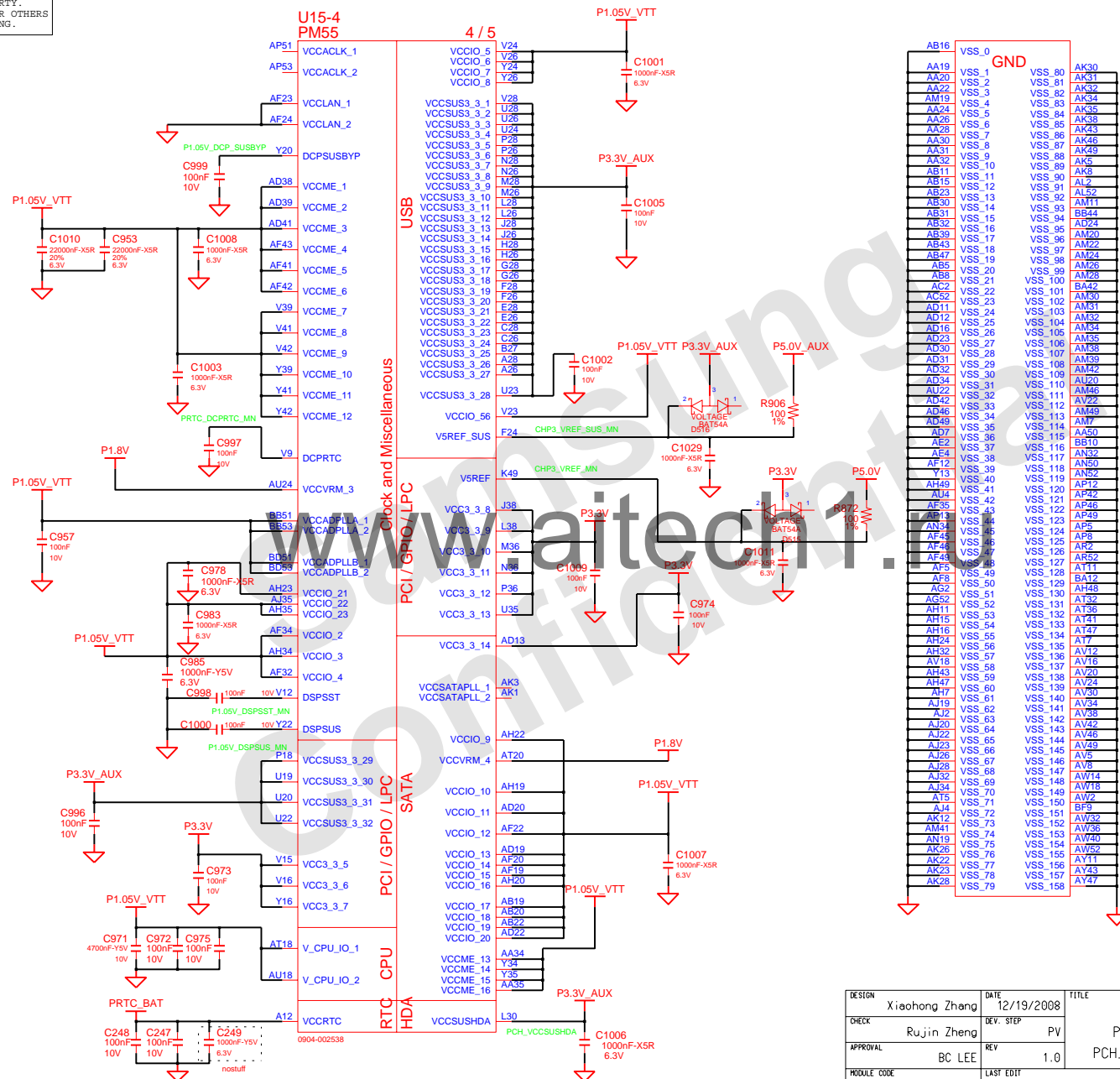
DESIGN	Xiaohong Zhang	DATE	12/19/2008	TITLE	Suzhou_M PCH_IBEAX PEAK PCH_IBEAX PEAK(1/6)	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	16 OF 62	

D:/users/ecad11/suzhou/tmp/ADV2/suzhou_n_py_1008



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P1.1V,P1.1V M is P1.05V & P1.05V M ACTUALLY

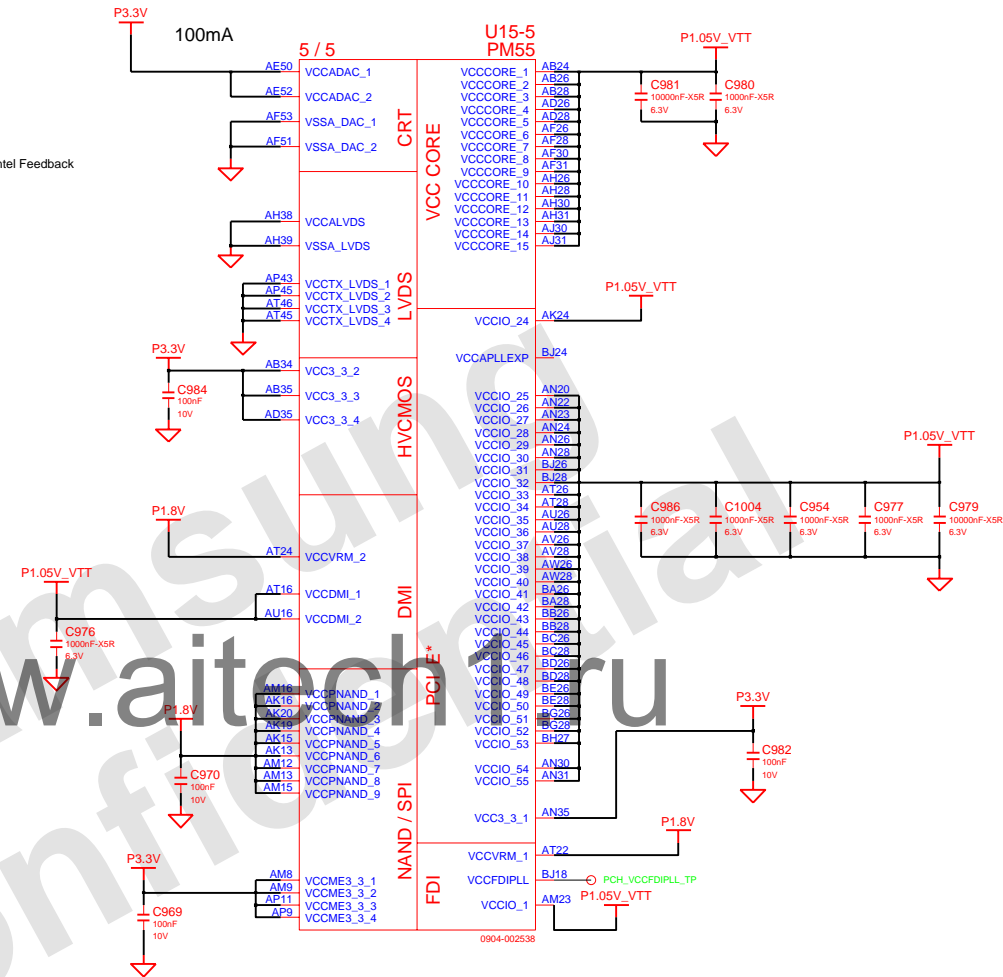


DESIGN	Xiaohong Zhang	DATE	12/19/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PCH_IBEAX PEAK		
APPROVAL	BC LEE	REV	1.0	PCH_IBEAX PEAK(4/6)	PART NO	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	19 OF 62	

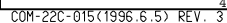
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H49	VSS_259	VSS_159	AY7
H5	VSS_260	VSS_160	B11
J24	VSS_261	VSS_161	B15
K11	VSS_262	VSS_162	B19
K43	VSS_263	VSS_163	B23
K47	VSS_264	VSS_164	B31
K7	VSS_265	VSS_165	B35
L14	VSS_266	VSS_166	B39
L18	VSS_267	VSS_167	B43
L2	VSS_268	VSS_168	B47
L22	VSS_269	VSS_169	B7
L32	VSS_270	VSS_170	B12
L36	VSS_271	VSS_171	B16
L40	VSS_272	VSS_172	B20
M12	VSS_273	VSS_173	B24
M16	VSS_274	VSS_174	B28
M20	VSS_275	VSS_175	B32
M24	VSS_276	VSS_176	B36
M38	VSS_277	VSS_177	B40
M42	VSS_278	VSS_178	B44
M46	VSS_279	VSS_179	B48
M49	VSS_280	VSS_180	B52
M5	VSS_281	VSS_181	B56
M8	VSS_282	VSS_182	BC10
N24	VSS_283	VSS_183	BC14
N34	VSS_284	VSS_184	BC18
N38	VSS_285	VSS_185	BC22
N42	VSS_286	VSS_186	BC26
N46	VSS_287	VSS_187	BC30
P11	VSS_288	VSS_188	BC34
P15	VSS_289	VSS_189	BC38
P22	VSS_290	VSS_190	BC42
P30	VSS_291	VSS_191	BC46
P32	VSS_292	VSS_192	BC50
P34	VSS_293	VSS_193	BD0
P42	VSS_294	VSS_194	BD4
P45	VSS_295	VSS_195	BD8
P47	VSS_296	VSS_196	BD12
R12	VSS_297	VSS_197	BD16
R2	VSS_298	VSS_198	BD20
R52	VSS_299	VSS_199	BD24
T12	VSS_300	VSS_200	BD28
T41	VSS_301	VSS_201	BD32
T46	VSS_302	VSS_202	BD36
T49	VSS_303	VSS_203	BD40
T8	VSS_304	VSS_204	BD44
U30	VSS_305	VSS_205	BD48
U31	VSS_306	VSS_206	BD52
U32	VSS_307	VSS_207	BD56
U34	VSS_308	VSS_208	BD60
U38	VSS_309	VSS_209	BD64
V11	VSS_310	VSS_210	BD68
V16	VSS_311	VSS_211	BD72
V19	VSS_312	VSS_212	BD76
V20	VSS_313	VSS_213	BD80
V22	VSS_314	VSS_214	BD84
V30	VSS_315	VSS_215	BD88
V31	VSS_316	VSS_216	BD92
V32	VSS_317	VSS_217	BD96
V34	VSS_318	VSS_218	BD100
V35	VSS_319	VSS_219	BD104
V43	VSS_320	VSS_220	BD108
V45	VSS_321	VSS_221	BD112
V46	VSS_322	VSS_222	BD116
V47	VSS_323	VSS_223	BD120
V49	VSS_324	VSS_224	BD124
V5	VSS_325	VSS_225	BD128
V7	VSS_326	VSS_226	BD132
V8	VSS_327	VSS_227	BD136
W2	VSS_328	VSS_228	BD140
W52	VSS_329	VSS_229	BD144
Y11	VSS_330	VSS_230	BD148
Y12	VSS_331	VSS_231	BD152
Y15	VSS_332	VSS_232	BD156
Y19	VSS_333	VSS_233	BD160
Y23	VSS_334	VSS_234	BD164
Y28	VSS_335	VSS_235	BD168
Y30	VSS_336	VSS_236	BD172
Y31	VSS_337	VSS_237	BD176
Y32	VSS_338	VSS_238	BD180
Y38	VSS_339	VSS_239	BD184
Y43	VSS_340	VSS_240	BD188
Y46	VSS_341	VSS_241	BD192
P49	VSS_342	VSS_242	BD196
V5	VSS_343	VSS_243	BD200
V6	VSS_344	VSS_244	BD204
V8	VSS_345	VSS_245	BD208
P24	VSS_346	VSS_246	BD212
T43	VSS_347	VSS_247	BD216
AD51	VSS_348	VSS_248	BD220
AT8	VSS_349	VSS_249	BD224
AD47	VSS_350	VSS_250	BD228
Y47	VSS_351	VSS_251	BD232
AT12	VSS_352	VSS_252	BD236
AM6	VSS_353	VSS_253	BD240
AT13	VSS_354	VSS_254	BD244
AM5	VSS_355	VSS_255	BD248
AK45	VSS_356	VSS_256	BD252
AK39	VSS_357	VSS_257	BD256
AV14	VSS_358	VSS_258	BD260

By design guide rev0.8 & Intel Feedback

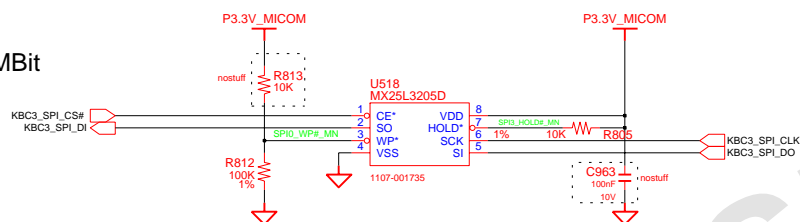


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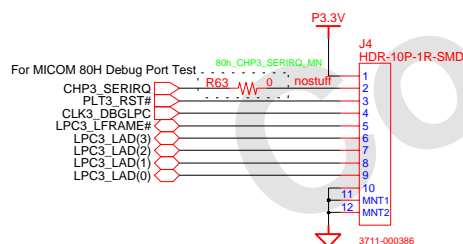
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16MBit



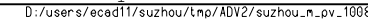
www.aitech

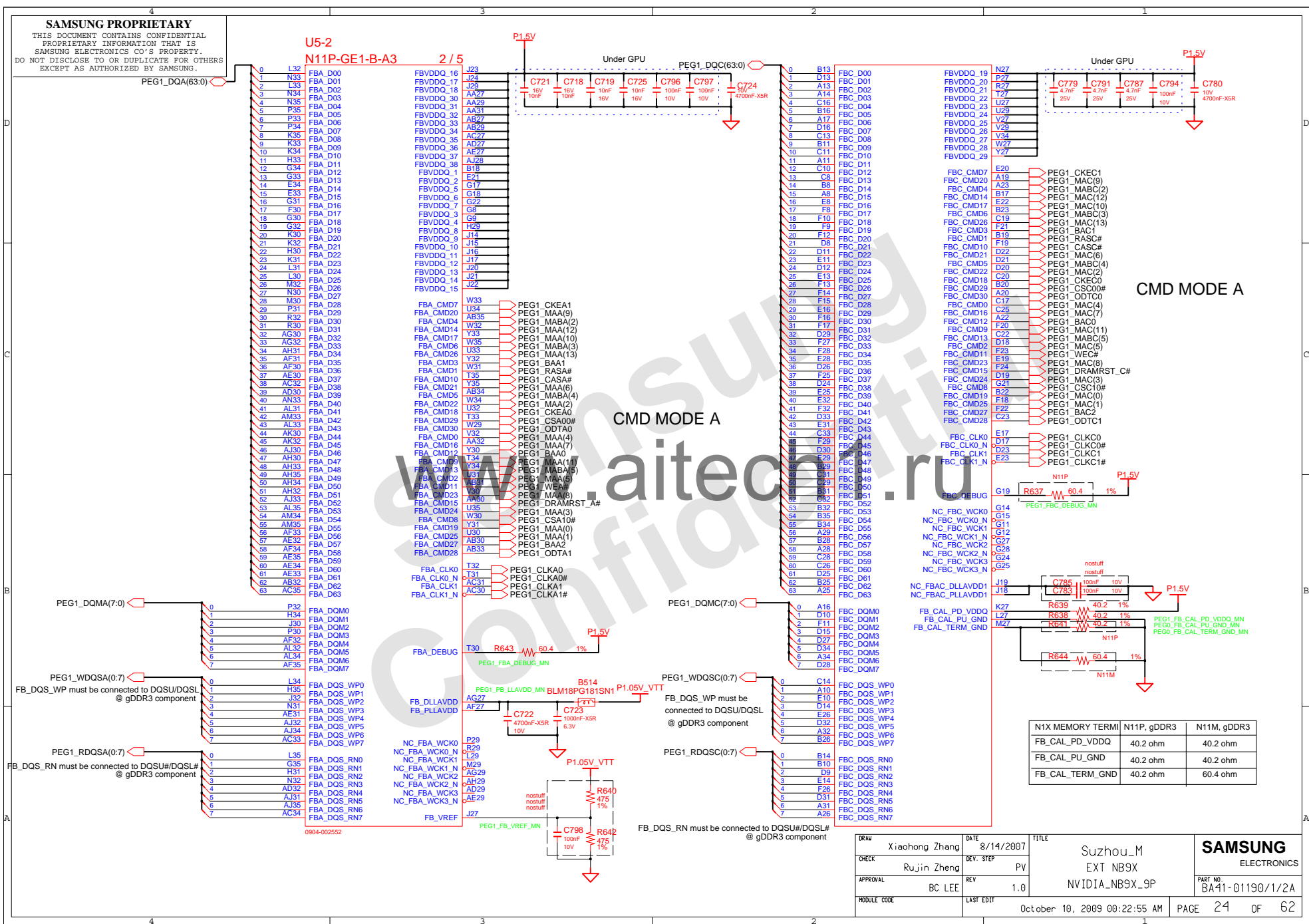
80H DECODER CONNECTOR



02	VERIFY REAL MODE	56	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT. CACHE TO POST	7E	TEST COPROCESSER INTERRUPT VECTOR
0E	INIT. I/O VALUE	7F	TEST COPROCESSER IF PRESENT
0F	ENABLE THE S-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA AREA
	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
18	8254 TIMER INIT	9C	SETUP POWER MANAGEMENT
19	8257 DMA CONTROLLER INIT.	9E	INIT. HARDWARE INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPOMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ACPI INIT
28	AUTO SIZING DRAM	AE	CHECK IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
36	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
38	AUTO SIZING CMOS	B6	ONE CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTER REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	BF	TEST CPU AND INT19
46	CHECK ROM COPY RIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I2O SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4B	INIT. AL VIDEO BIOS ROM	D8	SHUTDOWN 6 ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	89	ENABLE NMI
53	TEST KEYCLICK IF ENABLED	90	INIT. HDD CONTROLLER
54	ENABLE KEYBOARD	91	INIT. IDEAL IS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5A	DISPLAY / PRESS / SETUP	94	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 512K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
5D	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
5E	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

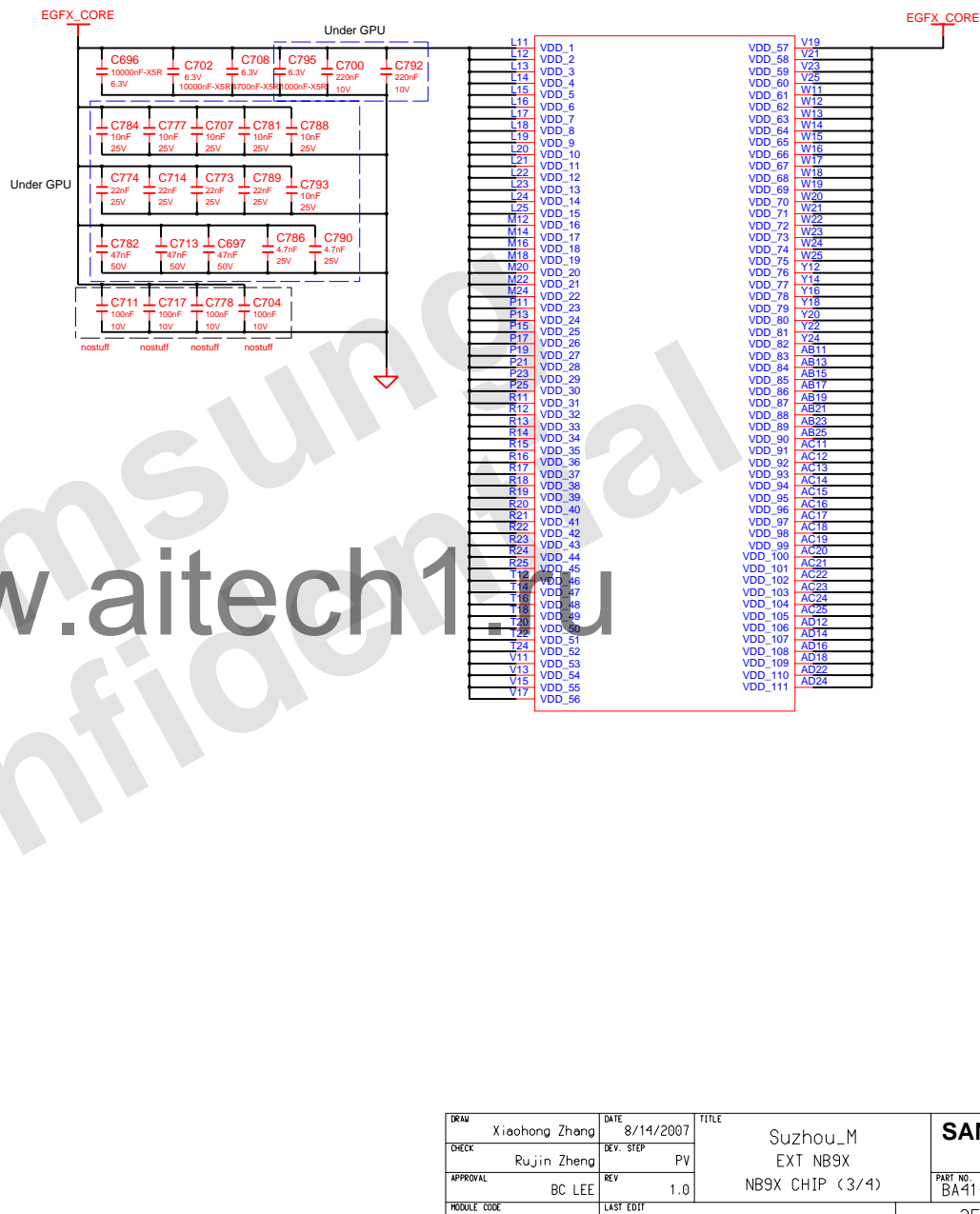
DRAW	Xiaohong Zhang	DATE	8/12/2006	TITLE	Suzhou_M	SAMSUNG	
CHECK	Rujin Zheng	DEV. STEP	PV		SPI_BIOS_ROM	ELECTRONICS	
APPROVAL	BC LEE	REV	1.0		SPI_BIOS_ROM	PART NO.	BA41-01190/1/2A
MODULE CODE	LAST EDIT			October 10, 2009 00:22:55 AM	PAGE	22	OF 62





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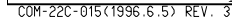
3 / 5



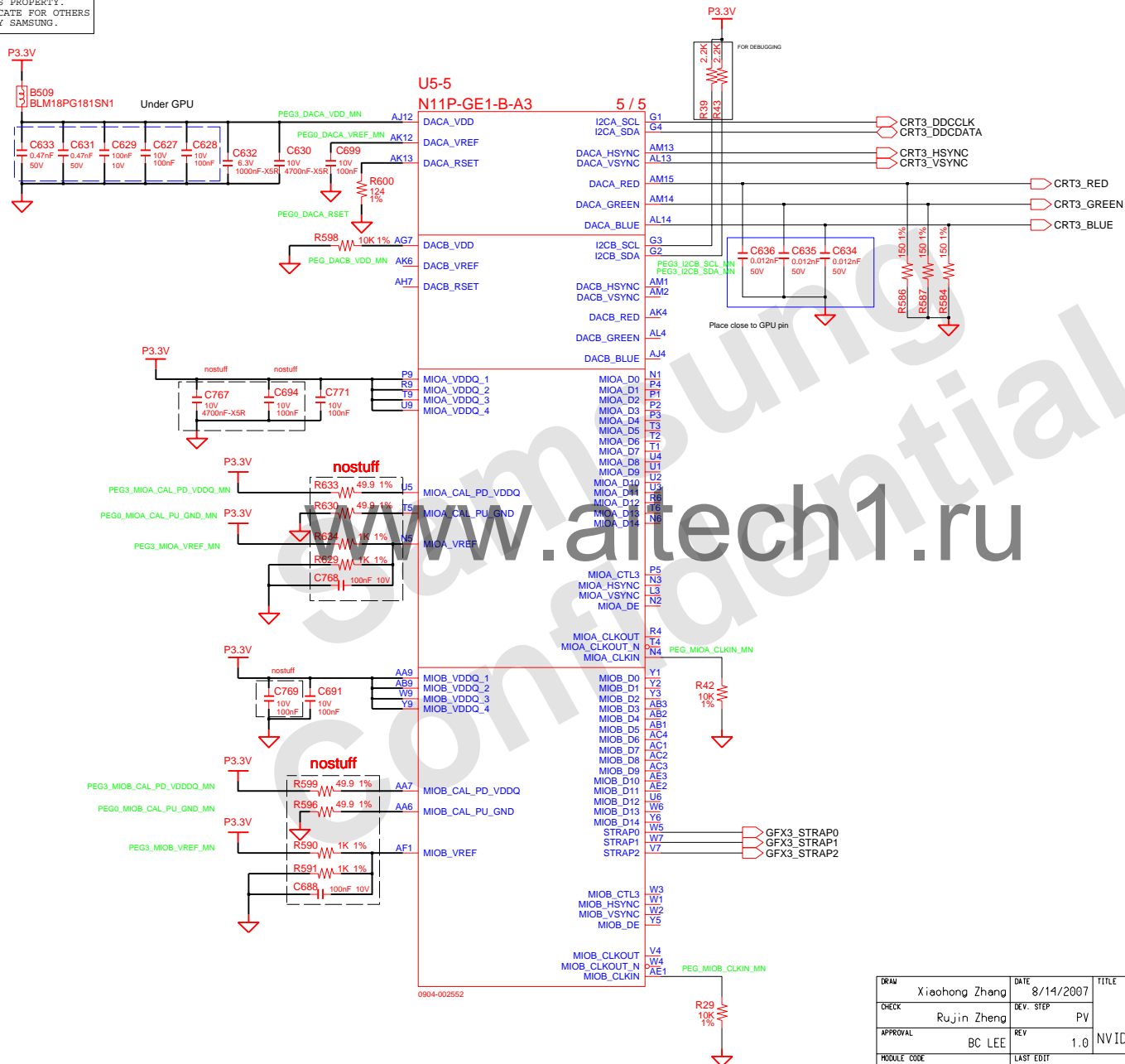
P1.05V_VTT

B508

BLM18PG181SN



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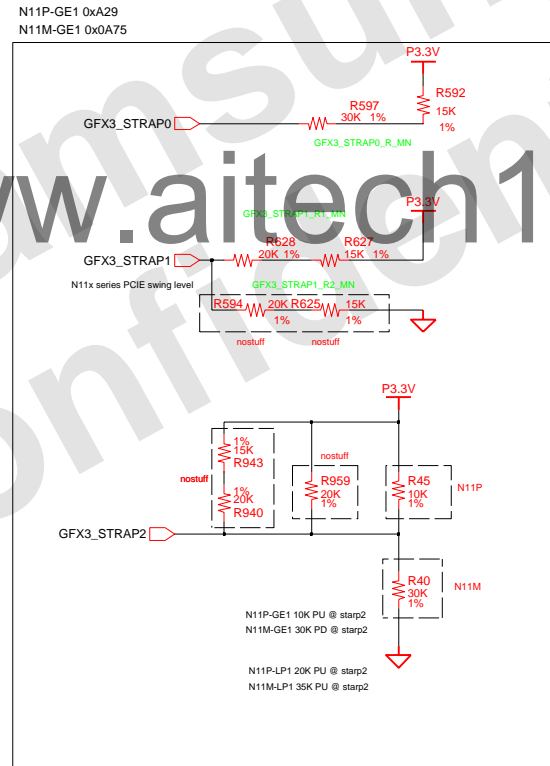
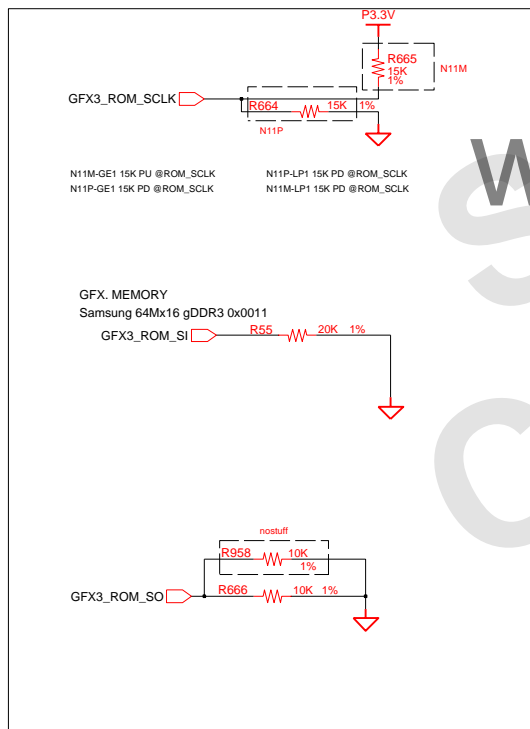
DRAW	Xiaohong Zhang	DATE	8/14/2007	TITLE	Suzhou_M EXT NB9X	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0	NVIDIA_NB9X_SP POWER RAIL	PART NO. BA41-01190/1/2A	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	27	OF 62

N11x_40nm STRAP

Pin	Description	Activate	Pin	Description	Activate
GPIO(0)	General Purpose	NC	GPIO(12)	PWR_LEVEL	NC
GPIO(1)	HPD-C	NC	GPIO(13)	MEM_VID	NC
GPIO(2)	LCD0_BL_PWM	High	GPIO(14)	PWR_CTRL1	NC
GPIO(3)	LCD0_VDD	High	GPIO(15)	HPD-E	High
GPIO(4)	LCD0_BL_EN	High	GPIO(16)	FAN_PWM	NC
GPIO(5)	GPU_VID0	00 0.8v 10 0.95v	GPIO(17)	Reserved	NC
GPIO(6)	GPU_VID1	01 0.85v 11 1.03v	GPIO(18)	Reserved	NC
GPIO(7)	GPU_VID2	NC	GPIO(19)	HPD-D	NC
GPIO(8)	OVERT	LOW			
GPIO(9)	ALERT	NC			
GPIO(10)	MEM_VREF	NC			
GPIO(11)	SLI_SYNC	NC			

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	1	0	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

N11P-GE1 0xA29

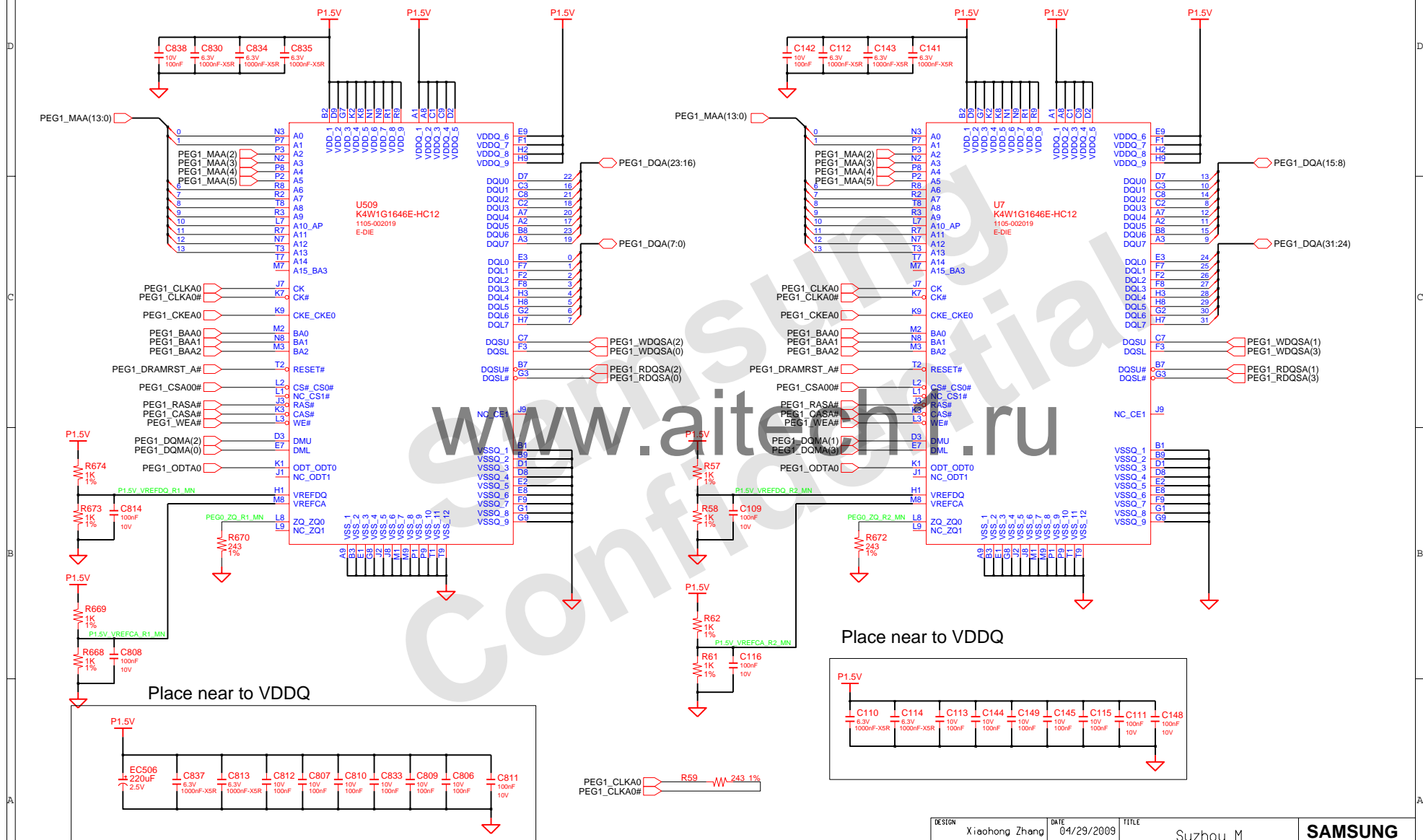
	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	0	1	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

N11M-GE1 0x0A75

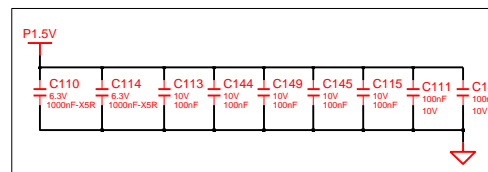
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A-Channel #0



Place near to VDDQ

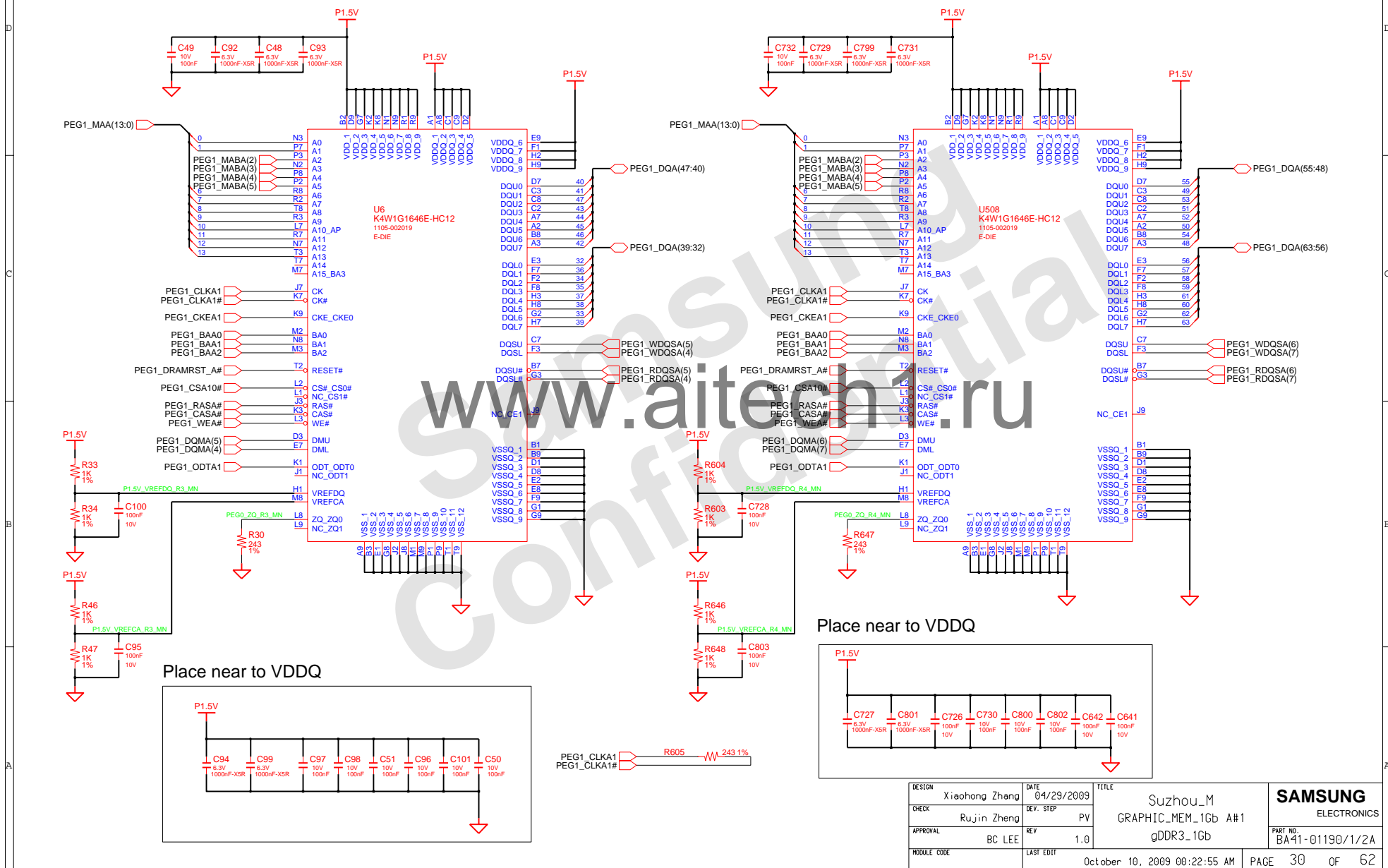


DESIGN	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHIC_MEM_1Gb A#0	
APPROVAL	BC LEE	REV	1.0	gDDR3_1Gb	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	29 OF 62

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ELECTRONICS

PART NO.
BA41-01190/1/2A

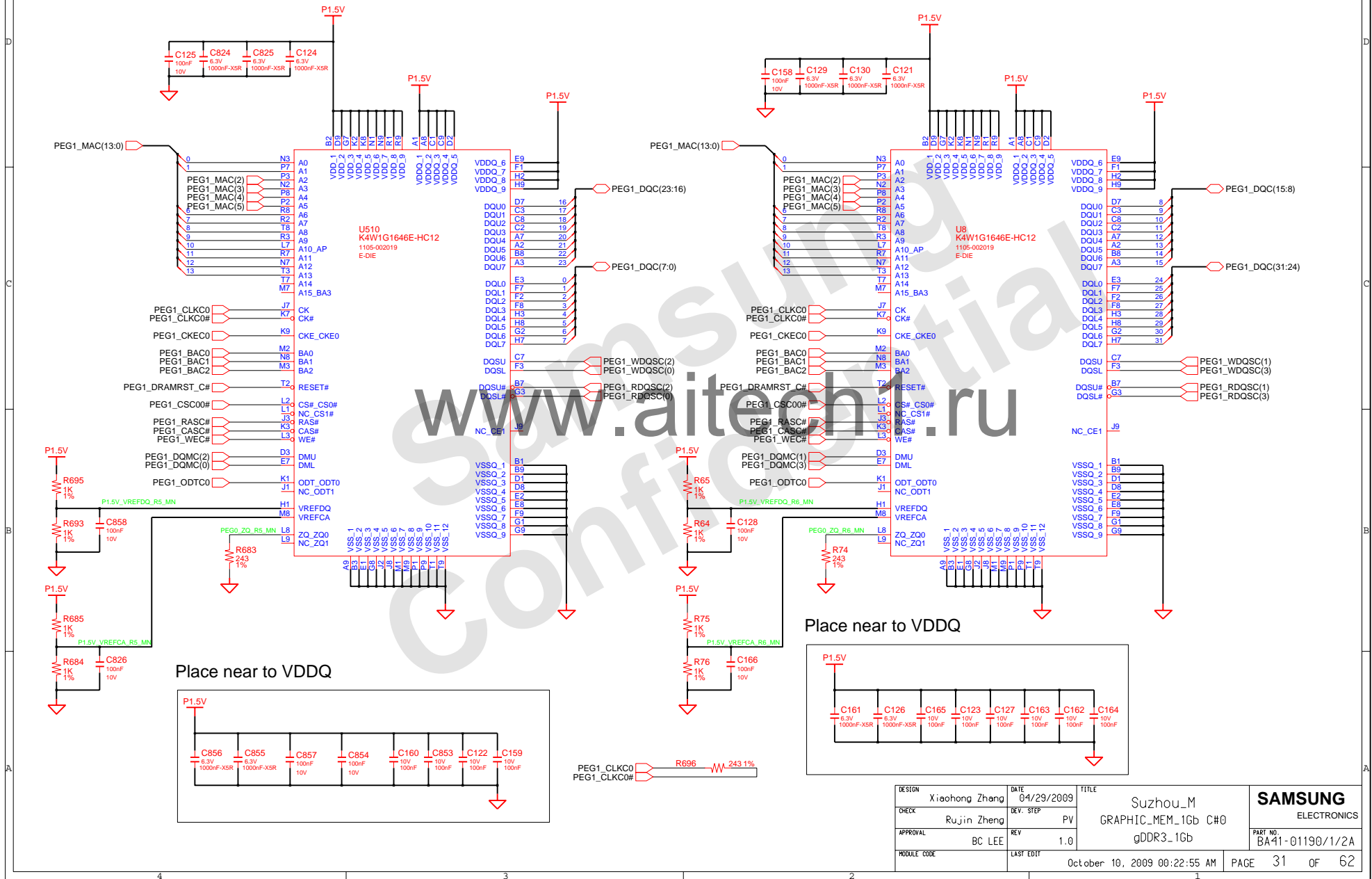
A-Channel #1



DESIGN	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV		GRAPHIC_MEM_1Gb A#1
APPROVAL	BC LEE	REV	1.0		gDDR3_1Gb
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	30 OF 62
				SAMSUNG ELECTRONICS	
				PART NO. BA41-01190/1/2A	

C-Channel #0

N11P

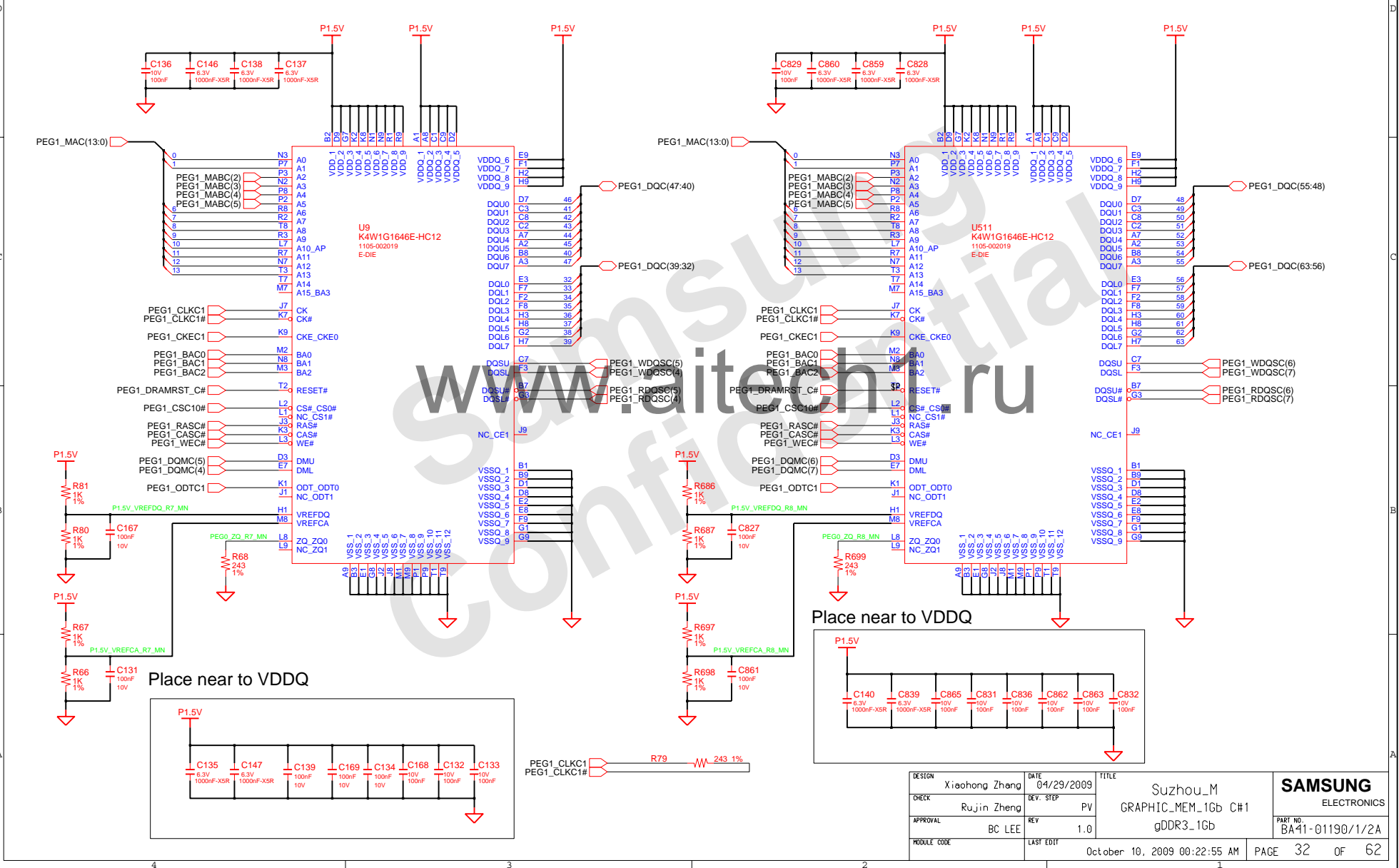


DESIGN	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHIC_MEM_1Gb C#0	
APPROVAL	BC LEE	REV	1.0	gDDR3_1Gb	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	31 OF 62

SAMSUNG
ELECTRONICS
PART NO.
BA41-01190/1/2A

C-Channel #1

N11P



DESIGN	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		GRAPHIC_MEM_1Gb C#1	
APPROVAL	BC LEE	REV	1.0		gDDR3-1Gb	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	32 OF 62	

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gDDR3 Memory PULL UP & PULL DOWN

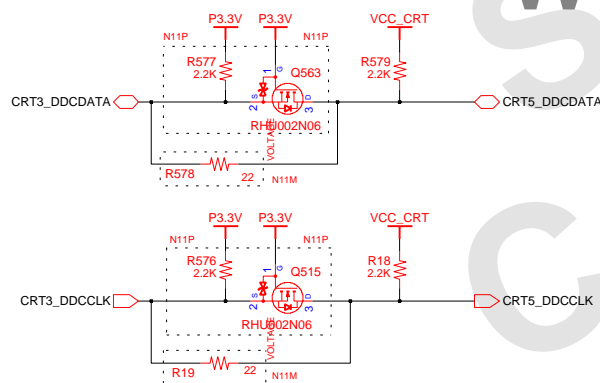
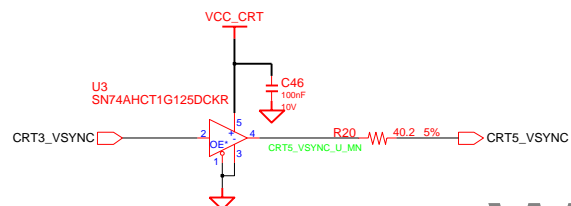
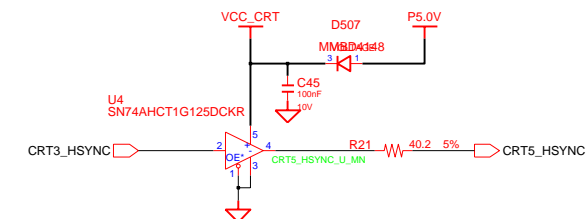


DESIGN	Xiaohong Zhang	DATE	03/14/2009	TITLE	Suzhou_M PULL-UP&PULL-DOWN gDDR3_1Gb	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 10, 2009 00:22:55 AM	PAGE 33	OF 62	

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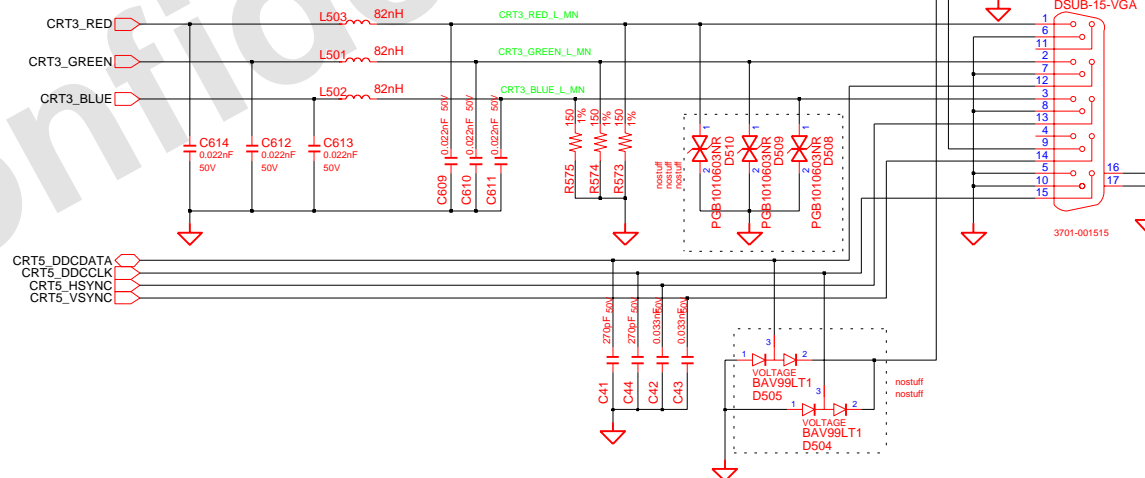
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CRT



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

CRT CONNECTOR

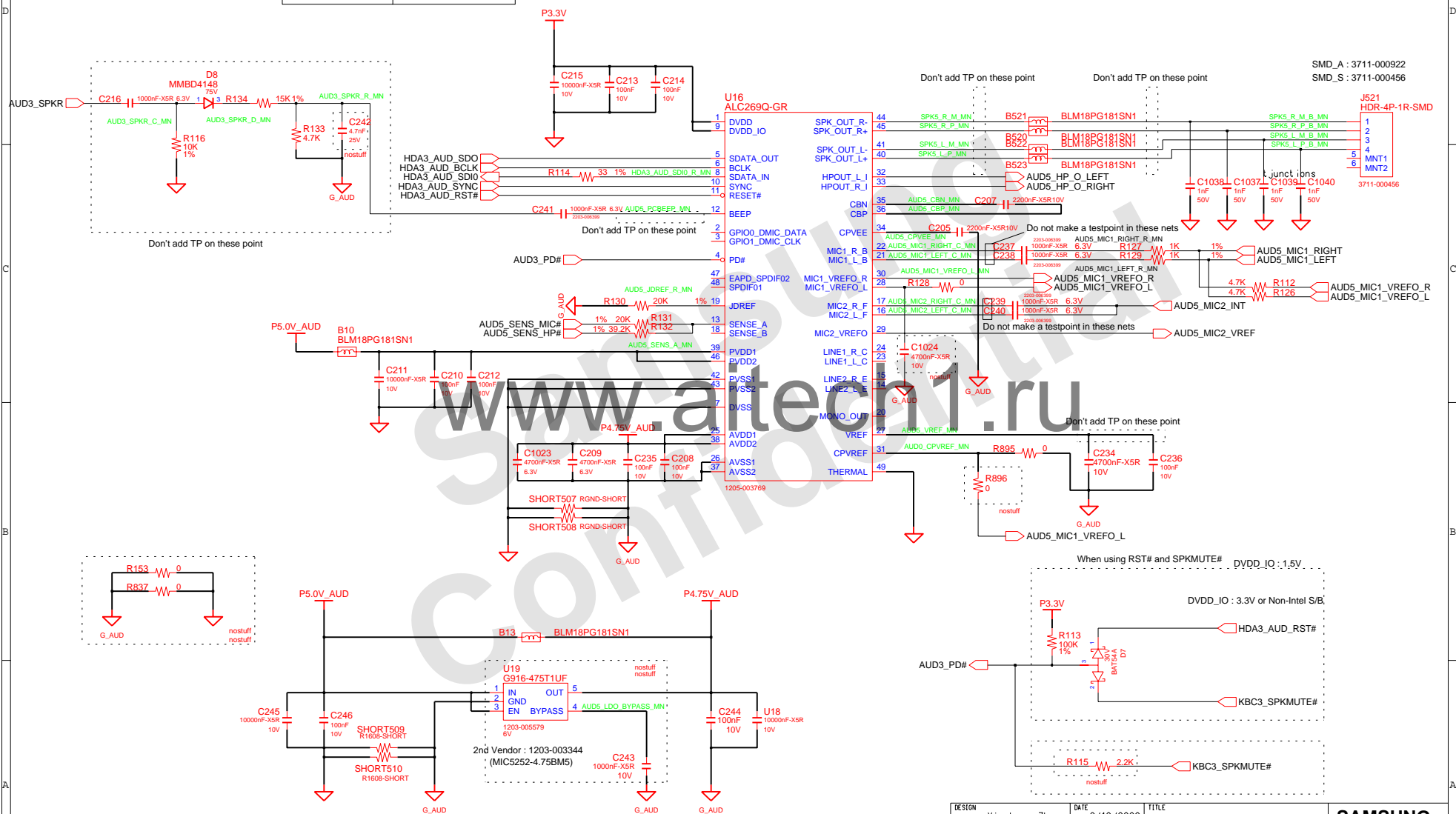


DESIGN	Xiaohong Zhang	DATE	01/08/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHICS_IF		
APPROVAL	BC LEE	REV	1.0	CRT		
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	34 OF 62	

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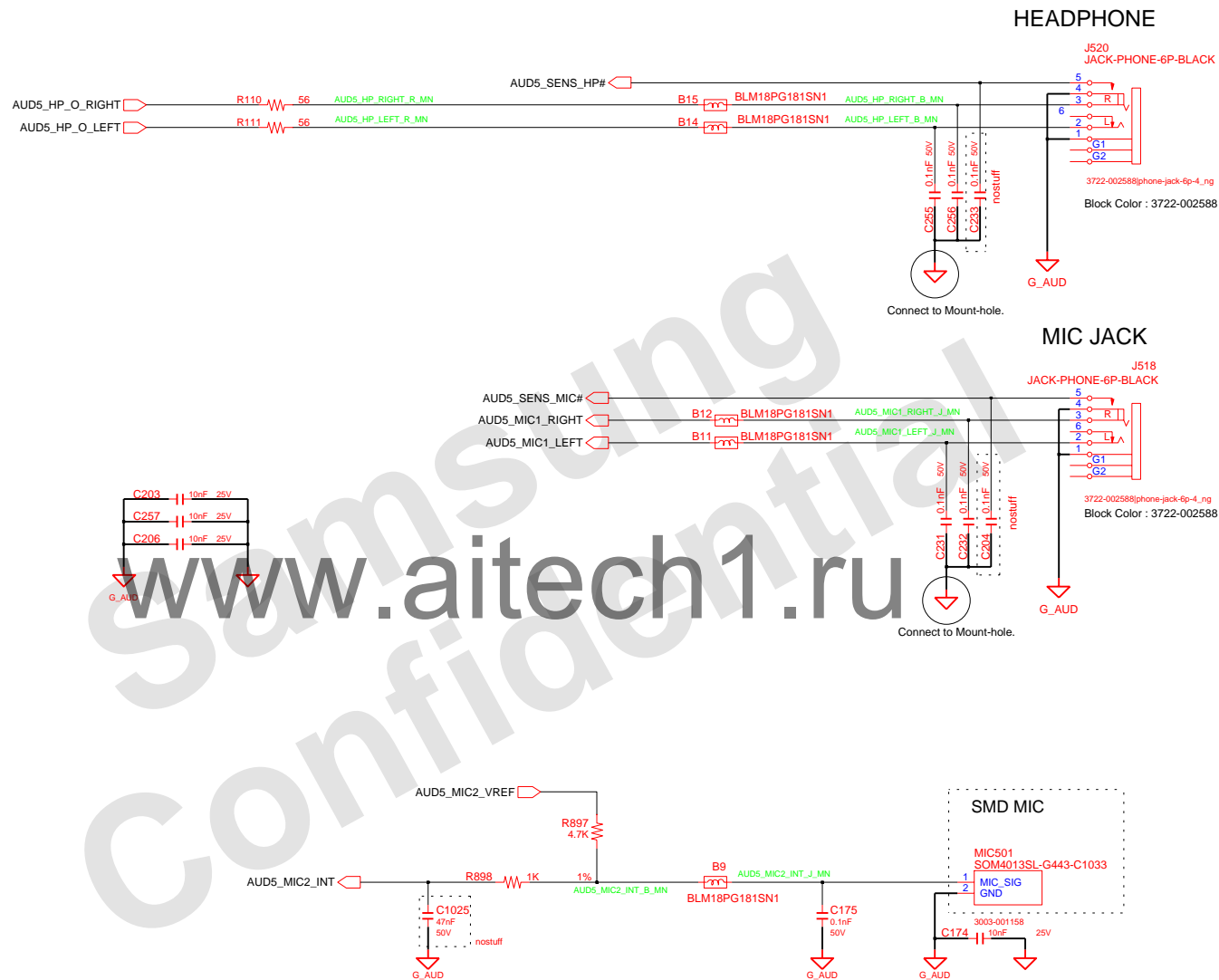
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



DESIGN	Xiaohong Zhang	DATE	3/13/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		HDA_ALC269_GR	
APPROVAL	BC LEE	REV	1.0		AUDIO CODEC	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	37 OF 62	

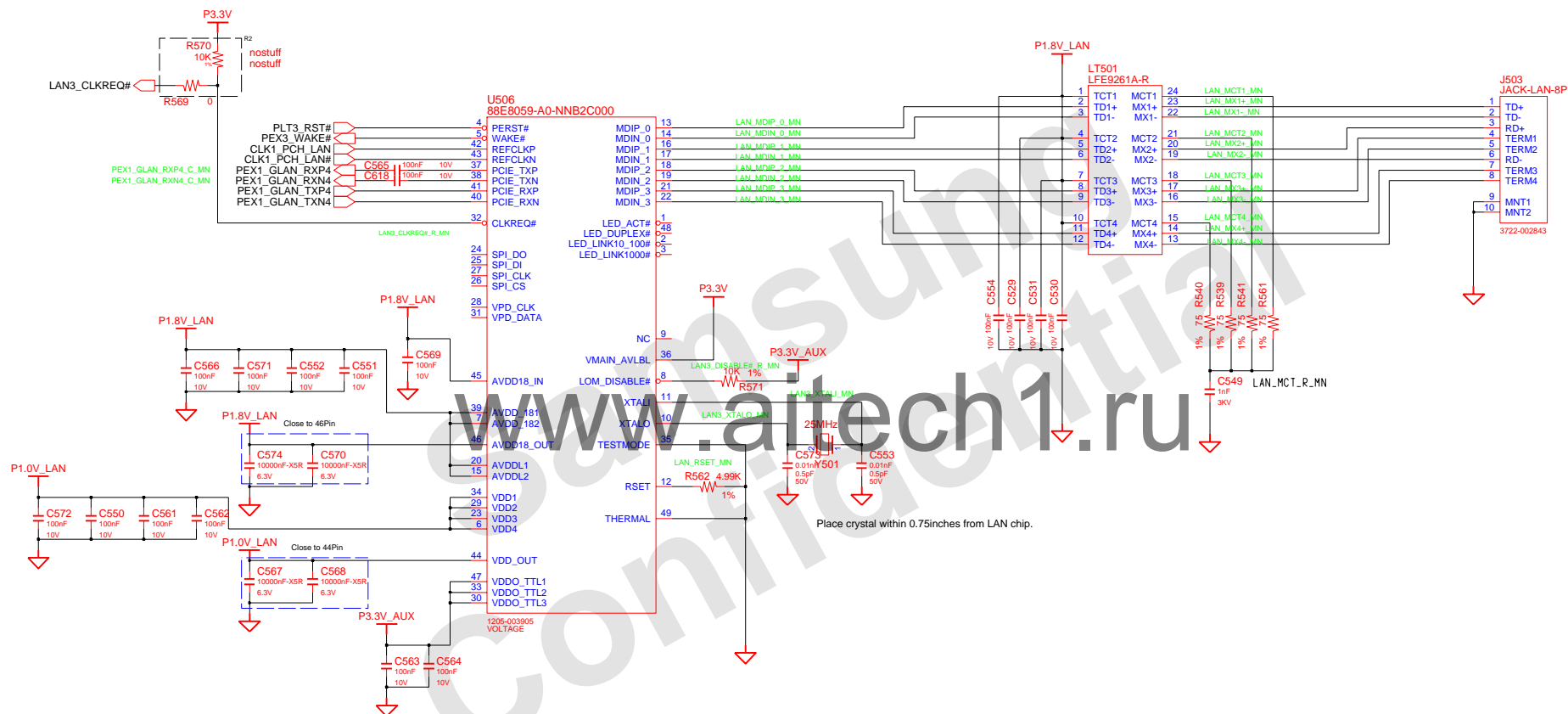
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DESIGN	Xiaohong Zhang	DATE	3/13/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		HDA_ALC269_GR	
APPROVAL	BC LEE	REV	1.0		AUDIO INPUT/OUTPUT	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	38 OF 62	

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DESIGN	Xiaohong Zhang	DATE	10/6/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 10, 2009 00:22:55 AM			
				PART NO.	BA41-01190/1/2A	

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The schematic shows the MDC interface circuit. It includes a J522 SOCK-12P-2R-SMD connector connected to a 3710-002193 component. The circuit features several signal pins: HDA3_MDC_SDO, HDA3_MDC_SYNC, HDA3_MDC_SD1#, and HDA3_MDC_RST#. A red resistor R937 (33 ohms, 5% tolerance) is connected between HDA3_MDC_SYNC and HDA3_MDC_SD1#. A green label indicates HDA3_MDC_SD1#_R_MIN. The circuit also includes a P3.3V_AUX power supply, capacitors C1045 (100nF, 10V) and C1044 (1000nF-XSR, 6.3V), and resistors R939 (10K), R938 (10K), and R936 (10K). A note "nostuff" is present near R936. A red cross symbol is located at the bottom right.

J511 HDR-2P-SMD

MNT2 4
MNT1 2

MDC48_TIP_B1_MN

MDC48_RING_B1_MN

3711-000541

To MDC card.

B7 B8

C1C21J801NE
C1C21J801NE

MDC48_TIP_B2_MN1

MDC48_RING_B2_MN1

C151 1nF 3KV

C117 1nF 3KV

MDC_GND

J508 JACK-MODEM-2P

RING TIP

MNT1 2
MNT2 4

* Basic : GND-No Connection
* EMI/ESD Issue : Connection

To RJ11 cable. (Connect with BA39-00593A)

3722-000246

MT509 RMINT-42-60-1P

MT519 RMINT-30-50-1P

MDC_GND

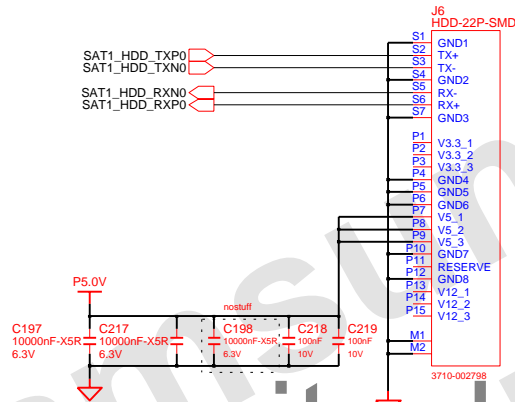
POWER

MDC_GND

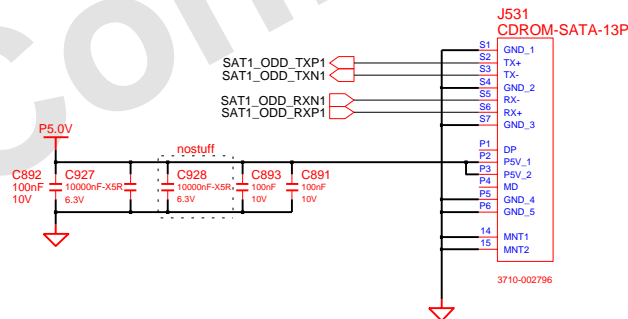
DESIGN	Xiaohong Zhang	DATE	8/20/2009	TITLE	Suzhou_M UNDEF INED UNDEF INED	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 10, 2009 00:22:55 AM			

SATA I/F CONN

SATA HDD CONN

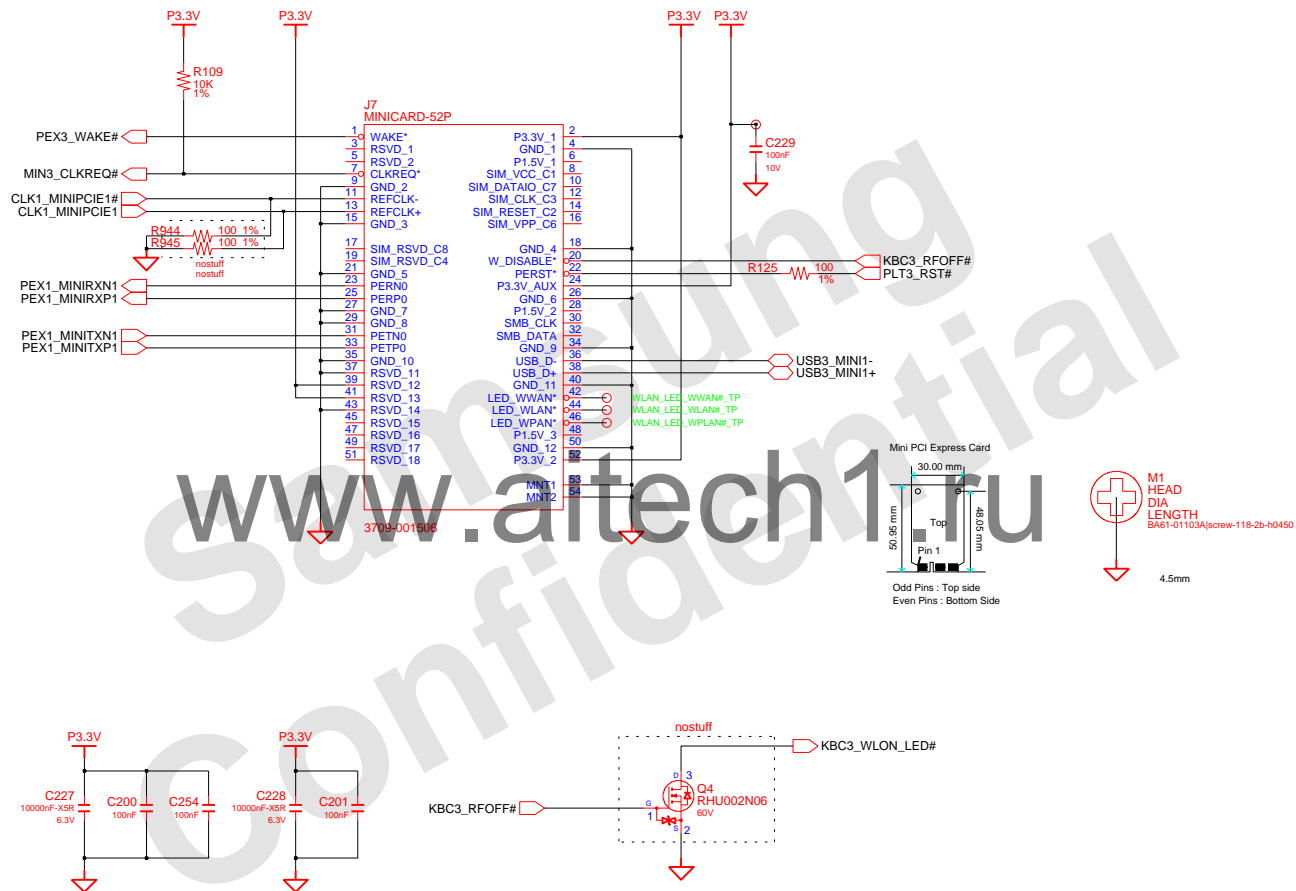


SATA ODD CONN



DESIGN	Xiaohong Zhang	DATE	6/6/2008	TITLE	Suzhou_M SATA_DEVICES	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	41 OF 62	

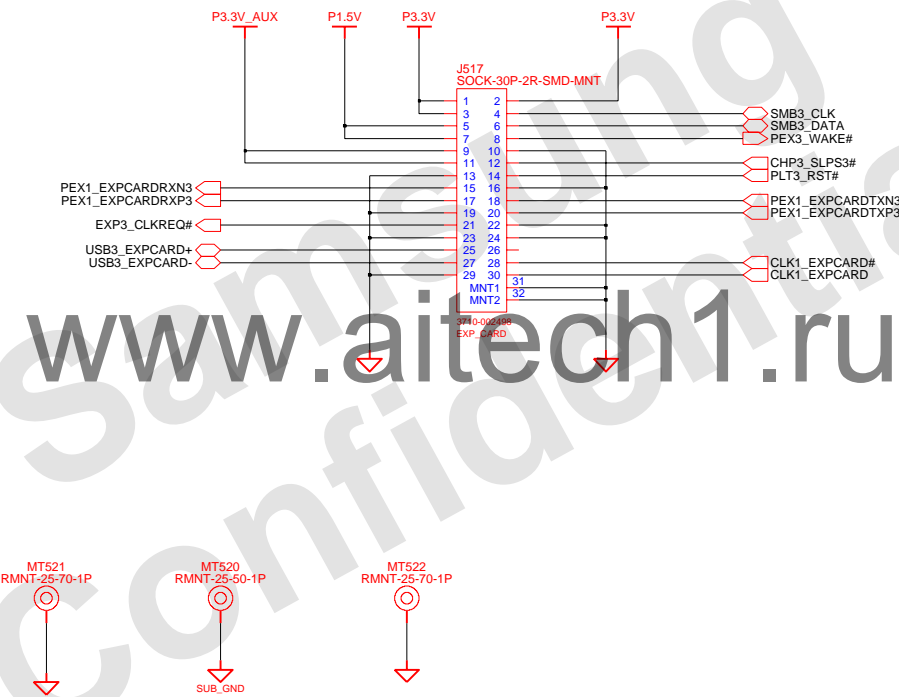
WLAN, 7mm



DESIGN	Xiaohong Zhang	DATE	6/6/2008	TITLE	Suzhou_M MINI_PCIE_CONN	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	42 OF 62	

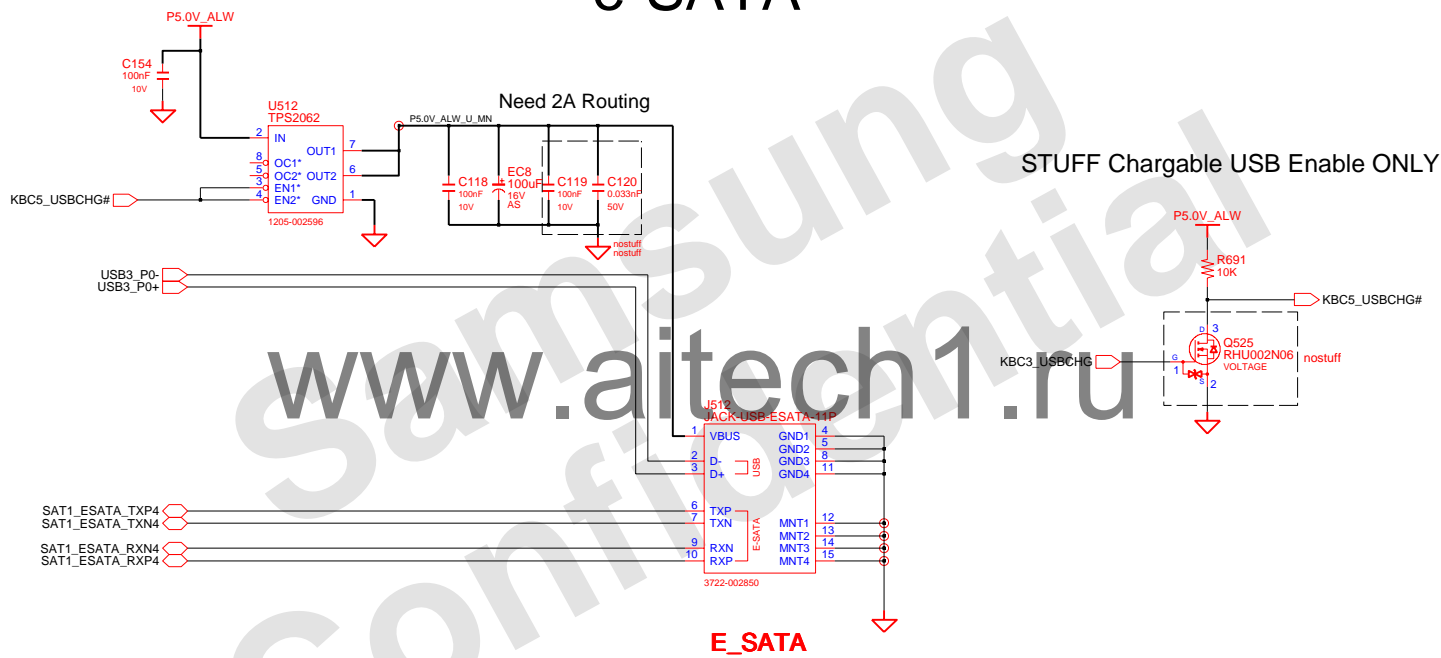
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Express Card

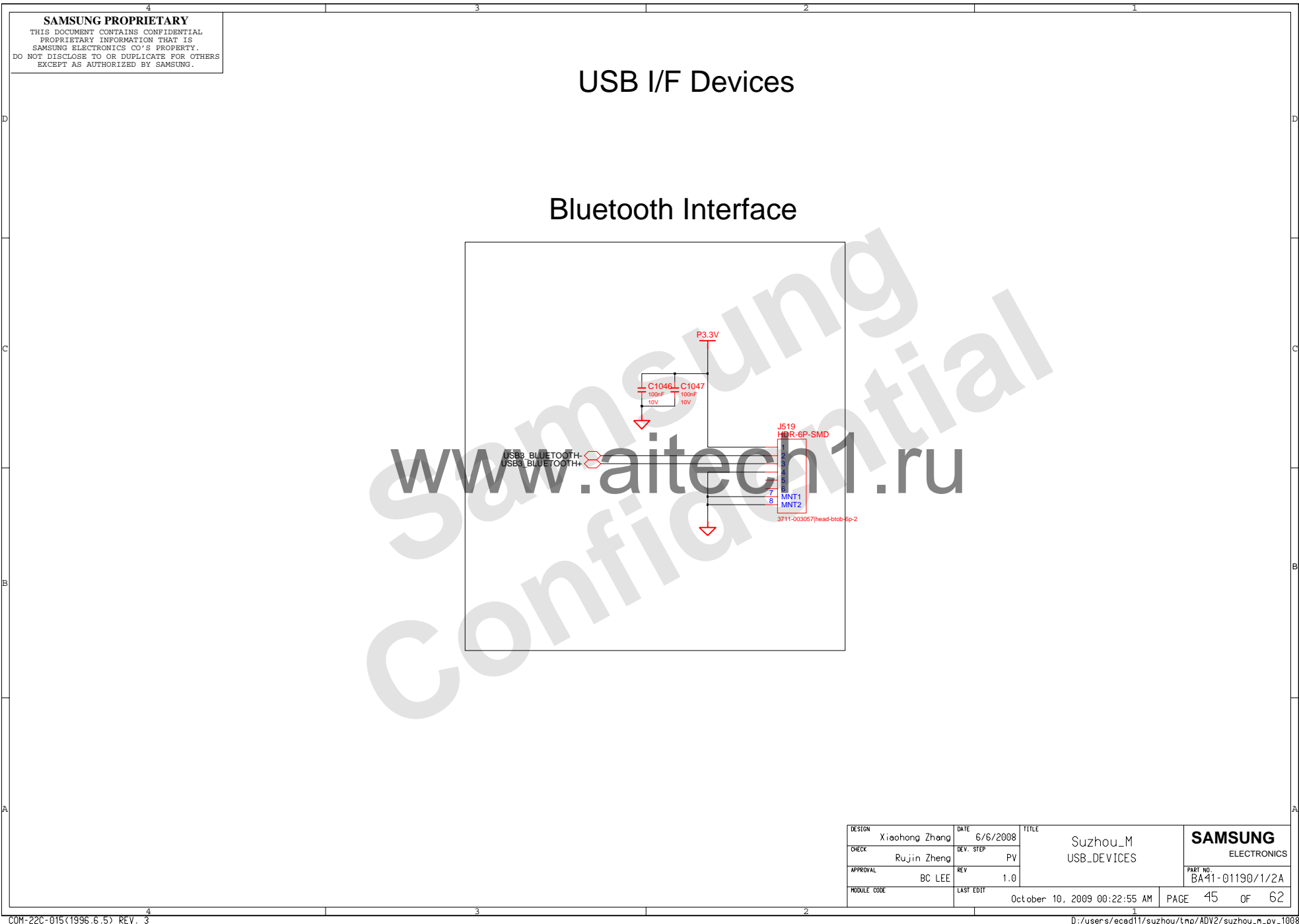


DESIGN	Xiaohong Zhang	DATE	7/7/2008	TITLE	Suzhou_M EXPRESS CARD	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	43 OF 62	

e-SATA



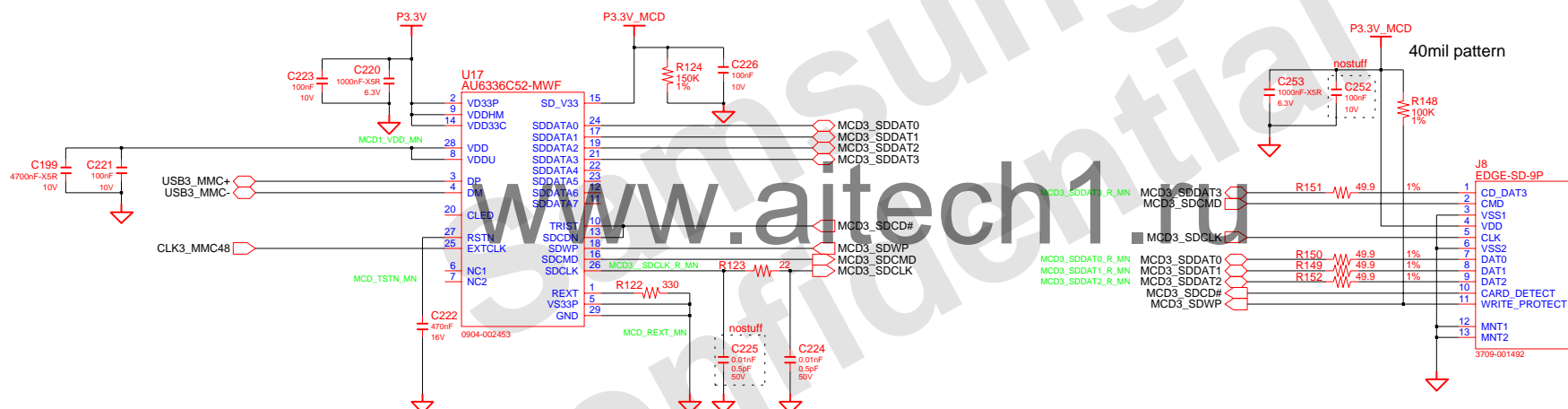
DRAW	Xiaohong Zhang	DATE	11/8/2006	TITLE	Suzhou_M MINI CARD SILOH & EBORN	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	44	OF 62



DESIGN	Xiaohong Zhang	DATE	6/6/2008	TITLE	Suzhou_M USB_DEVICES	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	45 OF 62	

3 IN 1

P3.3V MCD distance between R5U880 and socket should be less than 2 inches



40 mil trace for medica card socket ground

MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

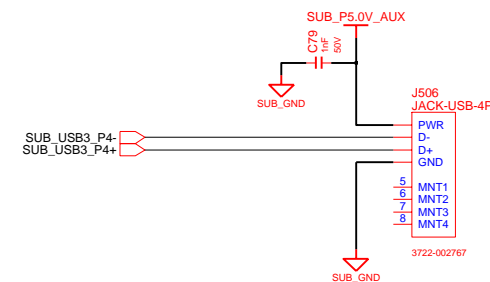
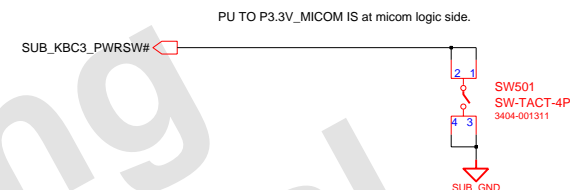
DESIGN	Xiaohong Zhang	DATE	10/15/2008	TITLE		Suzhou_M MMC AU6336		SAMSUNG ELECTRONICS	
CHECK	Rujin Zheng	DEV. STEP	PV						
APPROVAL	BC LEE	REV	1.0						
MODULE CODE		LAST EDIT		October 10, 2009 00:22:55 AM		PAGE	46	OF	62

Power Switch Button

19-217/T3D-AER1R2B5Y
LED501

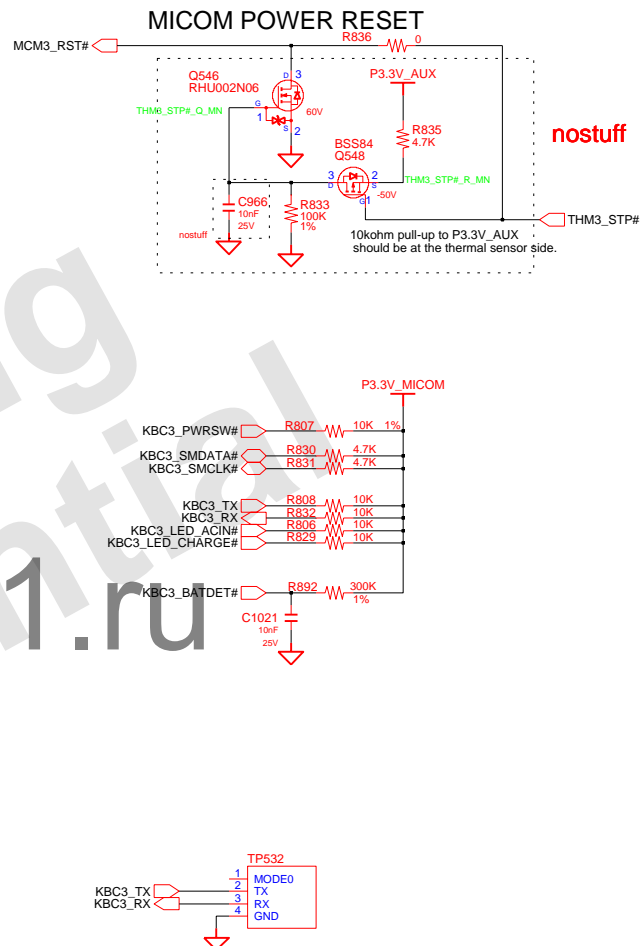
SY53_LED_POWER_MN R35 150 1% SUB P3.3V

Put this LED located near PWRSW from ME recommendation
Power LED, Blue color



D:/users/ecad11/suzhou/tmp/ADV2/suzhou_n_pv_1008

MAIN BOARD (MICOM)



D:/users/ecad11/suzhou/tmp/ADV2/suzhou_m_pv_1008

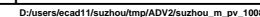
LED SWITCH LOGIC

Function Key LEDS

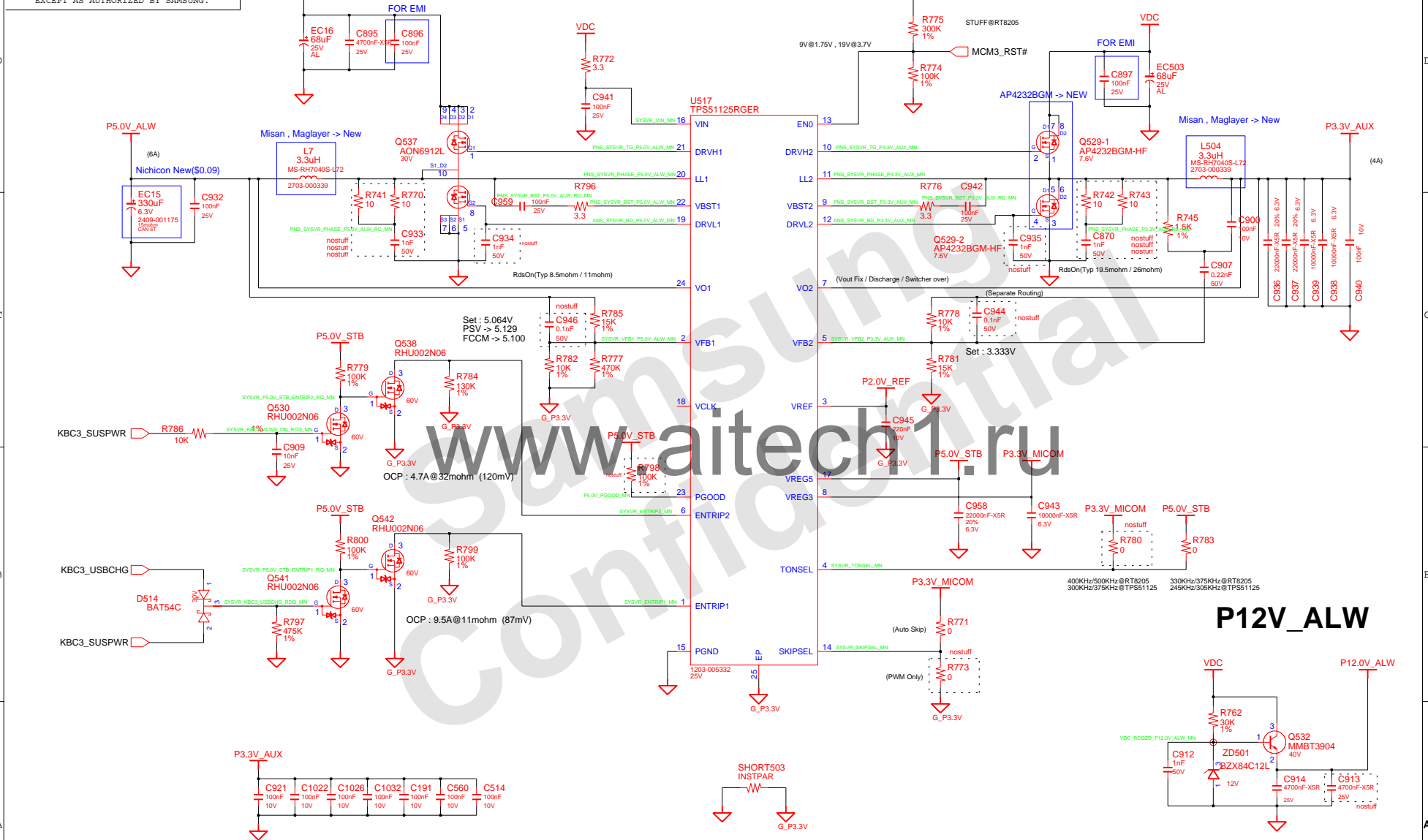


DRAW	Xiaohong Zhang	DATE	8/12/2006	TITLE	Suzhou_M	SAMSUNG
CHECK	Rujin Zheng	DEV. STEP	PV	LED_Switch	LED_Switch	ELECTRONICS
APPROVAL	BC LEE	REV	1.0	LED_Switch		PART NO.
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM			BA41-01190/1/2A
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CHARGER & POWER MANAGEMENT



P3.3V_AUX & P5.0V_ALW

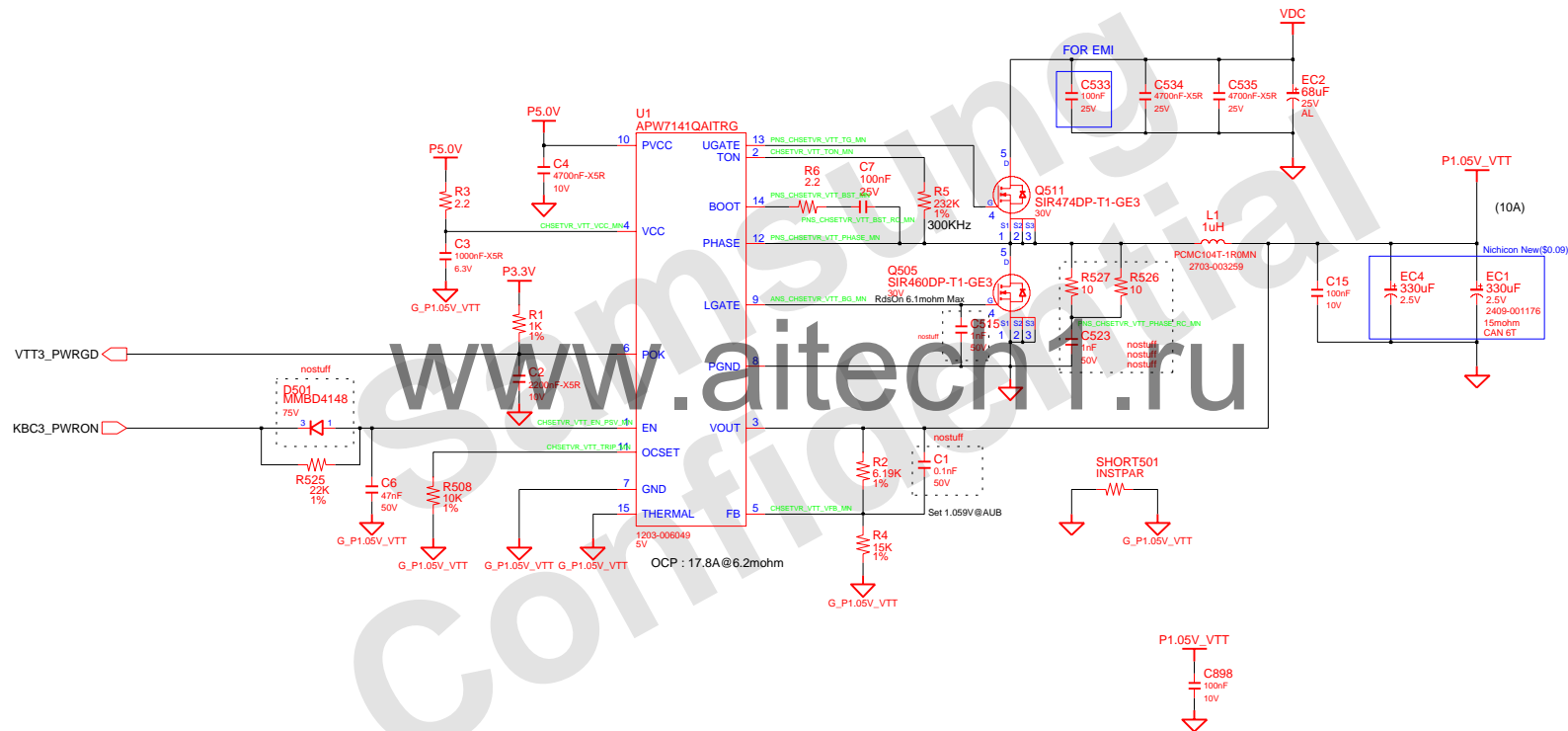


P12V_ALW

DRAW	Xiaohong Zhang	DATE	04/01/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		PWR_MV_3V_5V_Rt8205a	
APPROVAL	BC LEE	REV	1.0		P3.3V_AUX / P5.0V_AUX	
MODULE CODE	undefined	LAST EDIT				

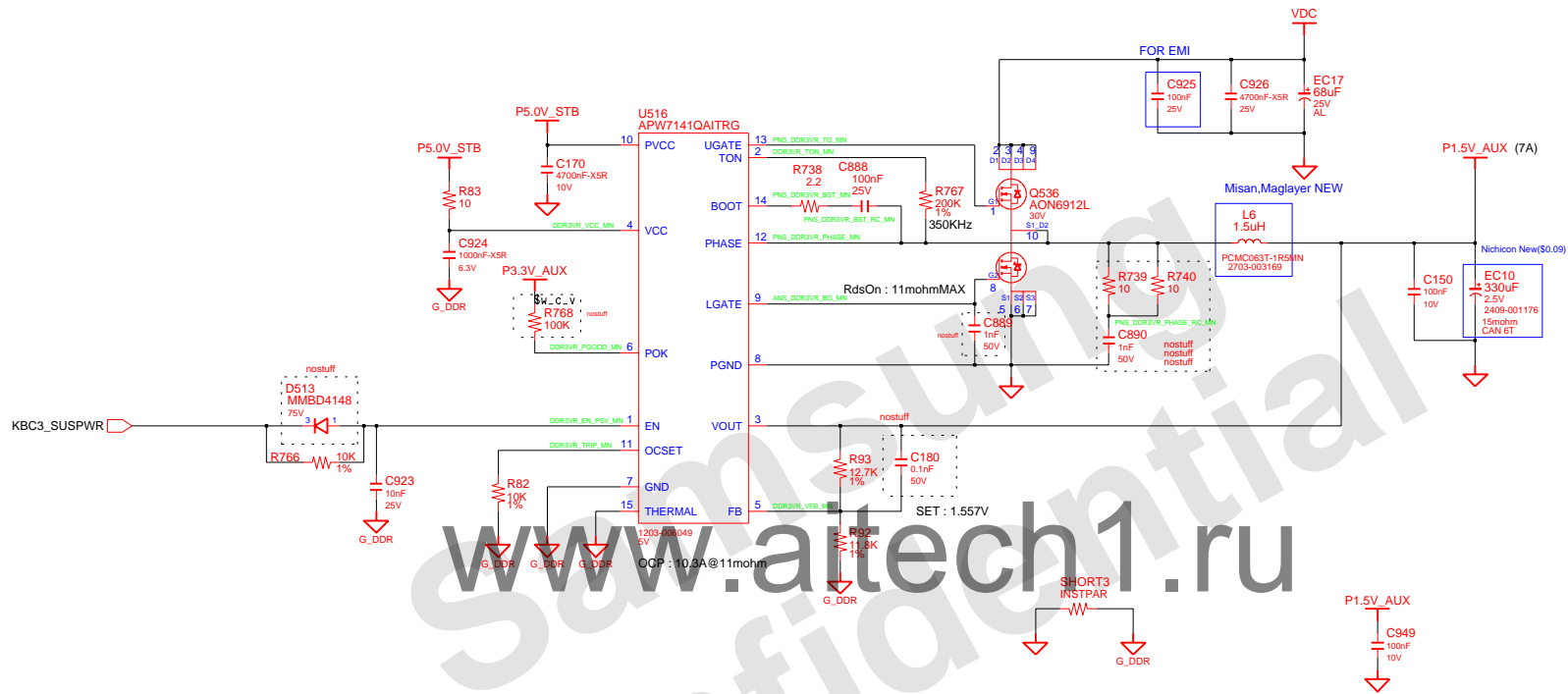
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CHIPSET POWER(P1.05V_VTT & P1.05V)

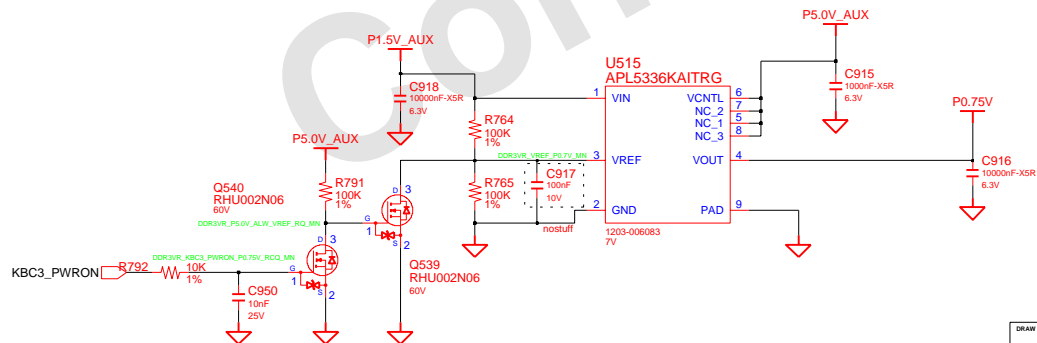


DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG
CHECK	Rujin Zheng	DEV. STEP	PV		PWR_MV_Cantiga	ELECTRONICS
APPROVAL	BC LEE	REV	1.0		Chipset Power (P1.05V_M,P1.2V)	PART NO.
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	53	BA41-01190/1/2A
				OF	62	

DDR3 Power



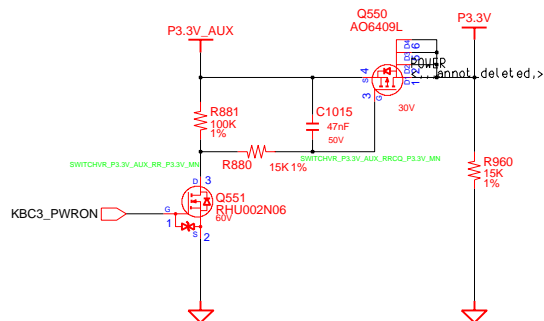
DDR3 VTT(0.75V)



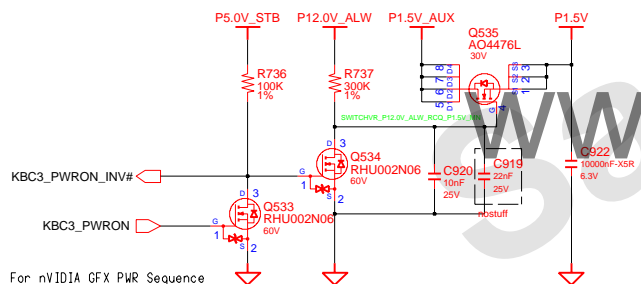
DRAW	Xiaohong Zhang	DATE	03/13/2009	TITLE	Suzhou_M	SAMSUNG
CHECK	Rujin Zheng	DEV. STEP	PV		PWR_MV_Memory_Rt8207	ELECTRONICS
APPROVAL	BC LEE	REV	1.0		DDR3 POWER (P1.5V_AUX)	PART NO.
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM			BA41-01190/1/2A
				PAGE	54	OF 62

Switched Power

Switched Power On (P3.3V)



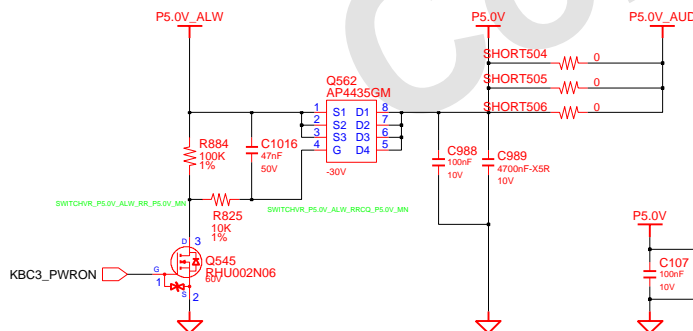
Switched Power On (P1.5V)



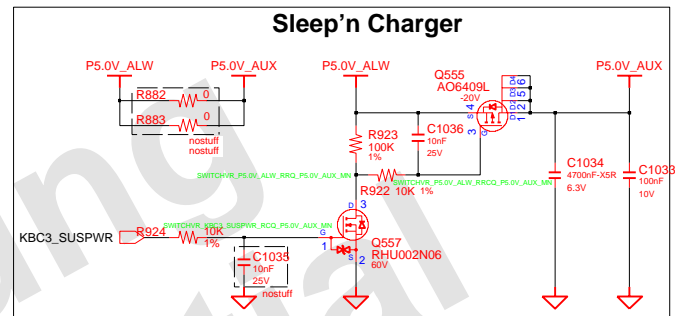
For nVIDIA GFX PWR Sequence

NVDD(EGFX_CORE) first and then FBVDD0(GDDR3)

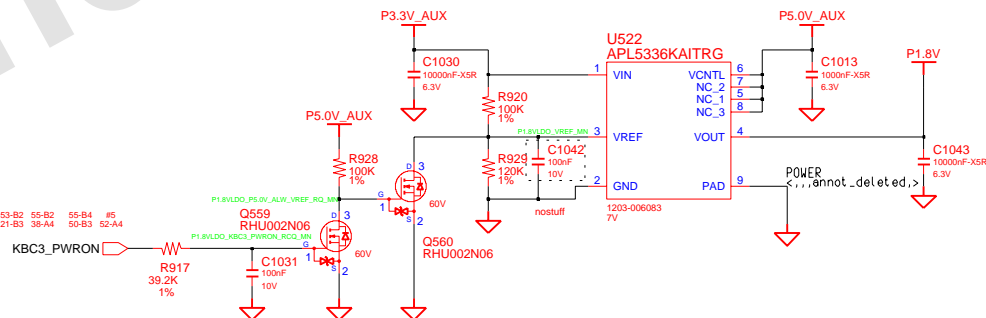
Switched Power On (P5.0V)



Sleep'n Charger



P1.8V(LDO)

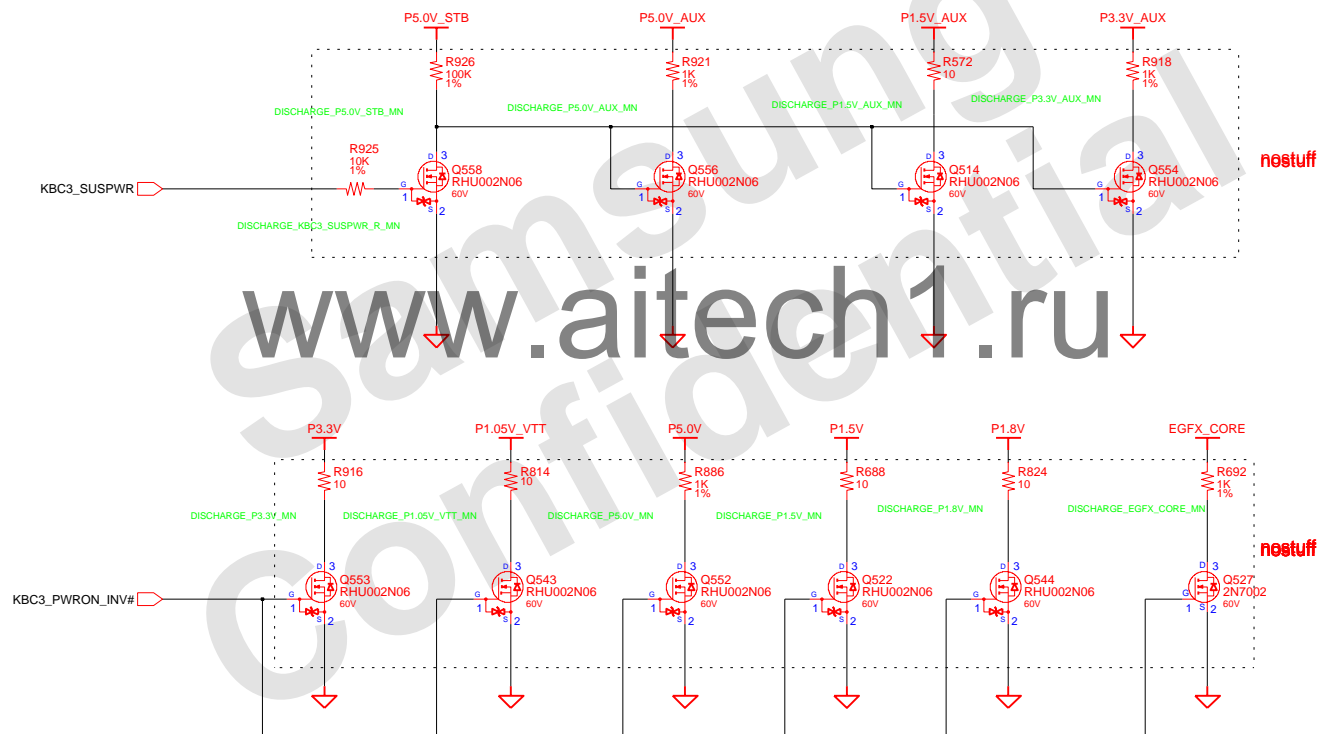


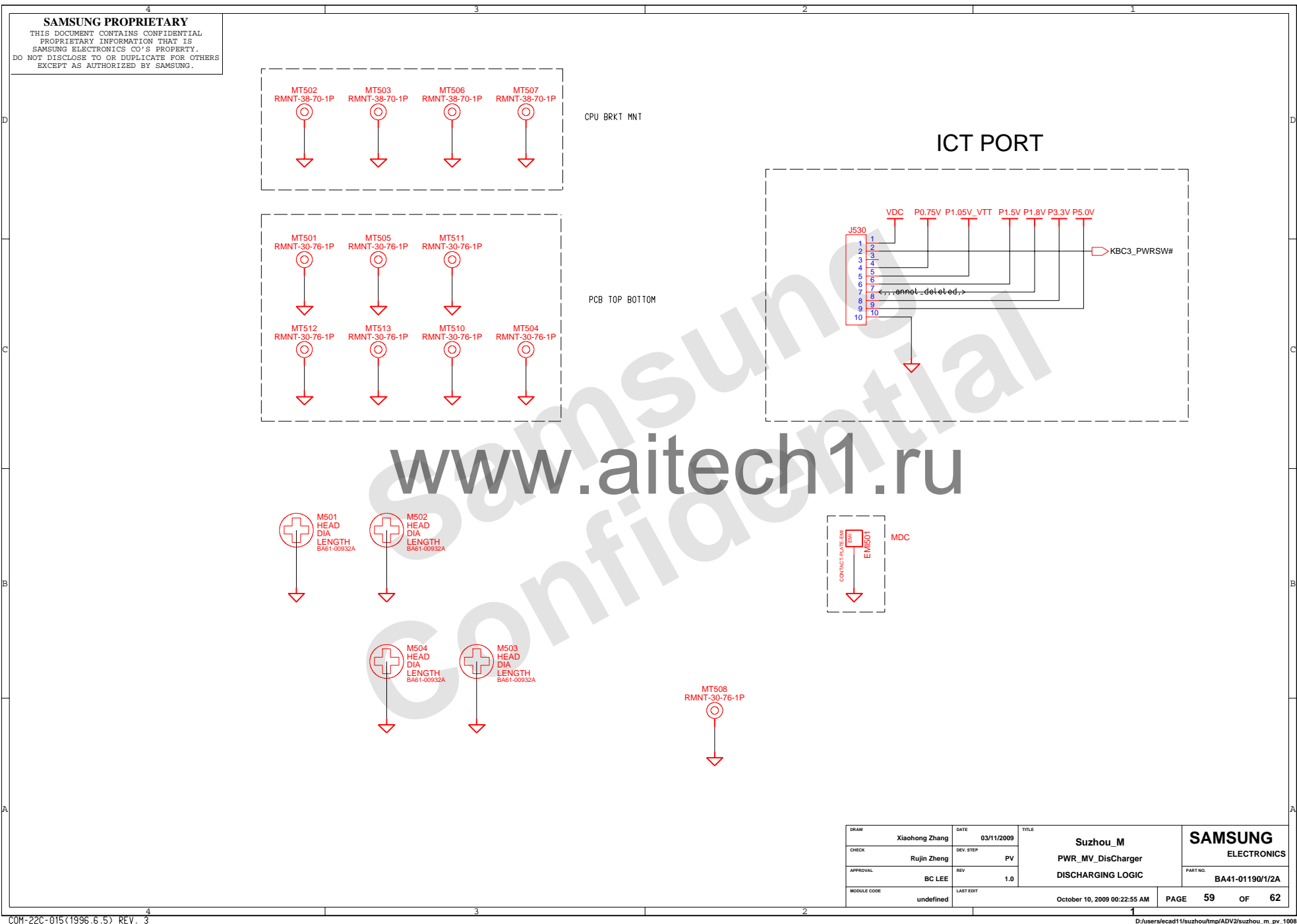
DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		PWR_MV_Switched	
APPROVAL	BC LEE	REV	1.0		SWITCHED POWER	
MODULE CODE		LAST EDIT				
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POWER DISCHARGER





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GPIO38
AUD3_PD#
FAN5_VDD
SMB3_CLK
SPI3_CLK
SPI3_CS#
ADT3_SEL#
AUD3_SPKR
CHP3_PECI
CPU1_PSI#
KBC3_A20G
KBC3_VRON
KBC5_TCLK
LCD3_BRIT
MCD3_SDWP#
MCM3_RST#
PLT3_RST#
SMB3_DATA
SPI3_MISO
SPI3_MOSI
CLK3_CHP14
CLK3_MMCA8
CRT3_GREEN
CRT3_HSYNC
CRT3_VSYNC
KBC3_CHGEN
KBC3_PWRGD
KBC3_PWRON
KBC3_RCI#
KBC5_TDATA
MCD3_SDCD#
MCD3_SDCLK
MCD3_SDCMD
PEX3_WAKE#
VTT3_PWRGD
AUD5_CBN_MN
AUD5_CBP_MN
CHP3_PMSYNC
CHP3_SERIRQ
CHP3_SLPS3#
CHP3_SLPS4#
CHP3_SLPS5#
CLK3_DBG_LPC
CLK3_PCI_FB
CPU1_VID(0)
CPU1_VID(1)
CPU1_VID(2)
CPU1_VID(3)
CPU1_VID(4)
CPU1_VID(5)
CPU1_VID(6)
CRT3_DDCCLK
GFX3_ROM_SI
GFX3_ROM_SO
GFX3_STRAP2
KBC3_BKLTON
KBC3_PWRSW#
KBC3_RFOFF#
KBC3_SMCLK#
KBC3_SPL_DI
KBC3_SPL_DO
KBC3_SUSPWR
KBC3_USBCHG
KBC5_KSI(0)
KBC5_KSI(1)
KBC5_KSI(2)
KBC5_KSI(3)
KBC5_KSI(4)
KBC5_KSI(5)
KBC5_KSI(6)
KBC5_KSI(7)
KBC5_KSO(0)
KBC5_KSO(1)

KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)
KBC5_KSO(8)
KBC5_KSO(9)
LAN_RSET_MN
LCD3_BKLTON
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
MCD3_SDDAT0
MCD3_SDDAT1
MCD3_SDDAT2
MCD3_SDDAT3
PEG3_BKLTON
SMB3_ALERT#
SPI3_WP#_MN
BAT3_DETECT#
CHP3_BATLOW#
CHP3_RTCRST#
CHP3_VREF_MN
CPU_TCK_R_MN
CRT3_DDCDATA
EGFXVR_EN_MN
EGFXVR_FB_MN
EXP3_CLKREQ#
FAN3_FDBACK#
GFX3_THERMON
GFX3_THERMDP
GFX3_VOLDI0
GFX3_VOLDI1
HDA3_AUD_SDO
HDA3_BCLK_MN
HDA3_MDC_SDO
KBC3_BATDET#
KBC3_CHG4.2V
KBC3_EXTSMI#
KBC3_PWRBTTN#
KBC3_RSMRST#
KBC3_RUNSCI#
KBC3_SMDATA#
KBC3_SPI_CLK
KBC3_SPI_CS#
KBC3_TX_J_MN
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KBC5_KSO(12)
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KBC5_KSO(14)
KBC5_KSO(15)
KBC5_USBCHG#
LAN3_CLKREQ#
LID3_SWITCH#
LPC3_LFRAME#
MEM3_CHB_SA0
MEM3_CHB_SA1
MNG3_CLKREQ#
PCH_GPIO0_MN
PCI3_CLKRUN#

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